The RISC-V Week
October 1st-3rd, 2019, Paris

Christian Fabre, CEA

- The 2nd RISC-V Meeting
  October 1st-2nd
  Espace Van Gogh, quai de la Rapée, Paris XII

- Scientific Day on RISC-V for Critical Embedded Systems
  October 3rd
  Campus de Jussieu, Paris V

Why the RISC-V Week?

- The 1st RISC-V Meeting was held on October 17th, 2018, in Grenoble
  - Academics only
  - On invitation only, both the audience and the speakers. Free.
  - 80 registered participants for 75 attending
  - Goal: have HW/SW people that could not cooperate on proprietary architectures talk together – and hopefully start working together.
- The 2nd RISC-V Meeting
  - In Paris,
  - Open to both industrial and academics
  - Speakers on invitation
  - More than 110 registration (+40% Y/Y)

Joint event with:

- GDR SCO2 Scientific Day on RISC-V for Critical Embedded System
  - Open to all
  - 80 registration – Limitation due to room capacity

The RISC-V Week

2nd RISC-V Meeting

- Tue. October 1st & Wed. 2nd
- 2 tutorials
- 3 keynotes
- 7 sessions of 1h: 3 talks of 15 min.

- Organized by
  - IRT Nanoelec, Grenoble
  - CEA
- Sponsored by
  - AdaCore, Rambus, Hensoldt

Scientific Day on RISC-V for Critical Embedded Systems

- Thu., October 3rd

- 7 Longer talks

- Organized by
  - IRT St-Exupéry, Toulouse
  - GDR SOC2 / CNRS

The goal of RISC-V Meeting is to bring new collaborations to life

- 2 tutorials
- 3 keynotes
- 7 sessions, each on a topic
  - 3 talks of 15 min. without Q&A
  - Q&A for the three speakers altogether

The 2nd RISC-V Meeting
Tuesday October 1st

- 10:00: Tutorial on RISC-V design using Free Open Source Software (Jean-Paul Chaput)
- 11:00 Break
- 11:30: Tutorial on Teaching basic computer architecture, assembly language programming, and operating system design using RISC-V (Frédéric Pétrot)
- 12:30: Lunch
- 13:30: Keynote from the RISC-V Foundation on The Momentum and Opportunity of Custom, Open Source Processing (Bertrand Tavernier)
- 14:30: Session on Open HW Opportunities (Chair: Thierry Collette)
- 15:30: Break
- 15:45: Session on Safe and Secure Computing with RISC-V (Chair: David Hely)
- 16:45: Break
- 17:00: Session on Modeling & Simulation (Chair: Frédéric Pétrot)
- 18:00: Closure

The 2nd RISC-V Meeting
Wednesday October 2nd

- 09:00 – Keynote on Uniprocessor Performance: It's the Instruction Fetch Front-End, Stupid! (André Seznec)
- 10:00 – Session: Towards High Performance (Chair: Kevin Martin)
- 11:00 – Break
- 11:30 – Session: Open Source Cores is an Actual Business (Chair: Yves Durand)
- 12:30 – Lunch
- 13:30 – Keynote on RISC-V in HPC: European Processor Initiative: challenges & opportunities for RISC-V accelerators in an HPC platform (Romain Dolbeau)
- 14:30 – Session on Improving the HW/SW Interface (Chair: Arnaud Tisserand)
- 15:30 – Break
- 16:00 – Session on Formal Verification (Chair: Olivier Savry)
- 17:00 – Presentation of the Scientific Day: RISC-V for critical embedded systems in Campus de Jussieu on Thursday October 3rd (Sébastien Faucou)
- 17:15 – Wrap-up on the 2nd RISC-V Meeting
- 17:30 – Closure

2nd RISC-V Meeting Committees

Program Committee

- Thierry Collette, Thales R&T
- Christian Fabre, CEA, chair
- Eric Flamand, GreenWaves Technologies
- Pierre Gobin, STMicroelectronics
- Nicolas Hili, IRT Saint-Exupéry
- David Hély, INPG/LCIS
- Mathieu Jan, CEA
- Kevin Martin, UBS/Lab-STICC
- Ivan Miró-Panadès, CEA
- Ahmed Ould El Hacen, Wisekey
- Thomas Peyret, CEA
- Frederic Pétrot, INPG/TIMA
- Olivier Savry, CEA, co-chair
- Olivier Sentieys, INRIA

Organization Committe

- Marion Andrillat, CEA
- Jean-Philippe Blanc, IRT Nanoelec
- Damien Couroussé, CEA
- Laurent-Frédéric Ducreux, IRT Nanoelec, co-chair
- Christian Fabre, CEA, chair
- Mathieu Jan, CEA
- Didier Louis, CEA
- Thomas Peyret, CEA
- Olivier Savry, CEA, co-chair
- Assia Tria, CEA

Sponsors of The 2nd RISC-V Meeting

AdaCore

Rambus

HENSOLDT
Detect and Protect.

RISC-V for Critical Embedded System Scientific Day Thursday October 3rd

- RISC-V in embedded applications (Michael Chapman, CORTUS)
- What does the space industry expect from RISC-V? (Antoine Certain, Airbus Defence & Space)
- Development of a RV64GC IP core for the GRLIB IP Library (Johan Klockars, Cobham Gaisler)
- European Processor Initiative: First steps towards a made-in-Europe high-performance microprocessor (Denis Dutoit, CEA Leti & EPI)
- Achieving determinism and performance on the RISC-V FlexPRET Processor (Eric Jenn, IRT Saint-Exupéry)
- RISC-V based Virtual Prototype: An Open Source Platform for Modeling and Verification (Daniel Große, University of Bremen & DFKI GmbH)
- Formal Verification of RISC-V Implementation Designs (Romain Soulat, Thales Research & Technology)

Misc.

- No food, no drinks in the conference room! Thanks
- PhD Students: Make sure to sign the *feuille d'émargement* each day to get a *certificat de présence* for your *école doctorale* curriculum
- Wifi:
  - SSID: auditorium
  - Password: espacevangogh
- Full program on posters outside the room