

# RISC-V design using FOSS

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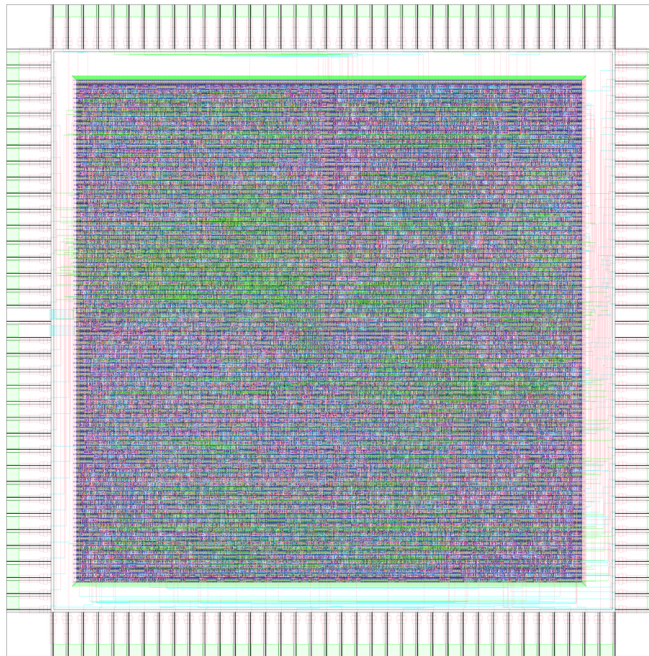
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# Plan

- 1 Goals
- 2 A First Try at RISC-V
- 3 Design Flow
- 4 Introduction to Symbolic Layout
- 5 Description of the Design Flow
- 6 Demo

# Goals



- Taking the next step for an open processor.
- Give the ability to publish, share and modify the hardware design down to the layout.
- Increase security.
- Ensure the continued existence of the hardware.

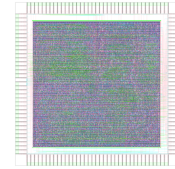
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# RISC-V design using FOSS

└ Goals

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Goals



- Taking the next step for an open processor.
- Give the ability to publish, share and modify the hardware design down to the layout.
- Increase security.
- Ensure the continued existence of the hardware.

- It seems only natural for a free and open processor to be built using free tools.
- By checking the layout, we can better detect hardware trojan and ensure the chip is exactly what it is.
- We expect FOSS to have the same effect of community building.
- NASA was forced to scavenge 8086 on eBay for the space shuttle around 2002.

# Implemented RISC-V ISA



- RV32I user-space ISA only.
- Target node will be AMS 350nm, 4 metal layers.

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## RISC-V design using FOSS

└─ A First Try at RISC-V

└─ Implemented RISC-V ISA

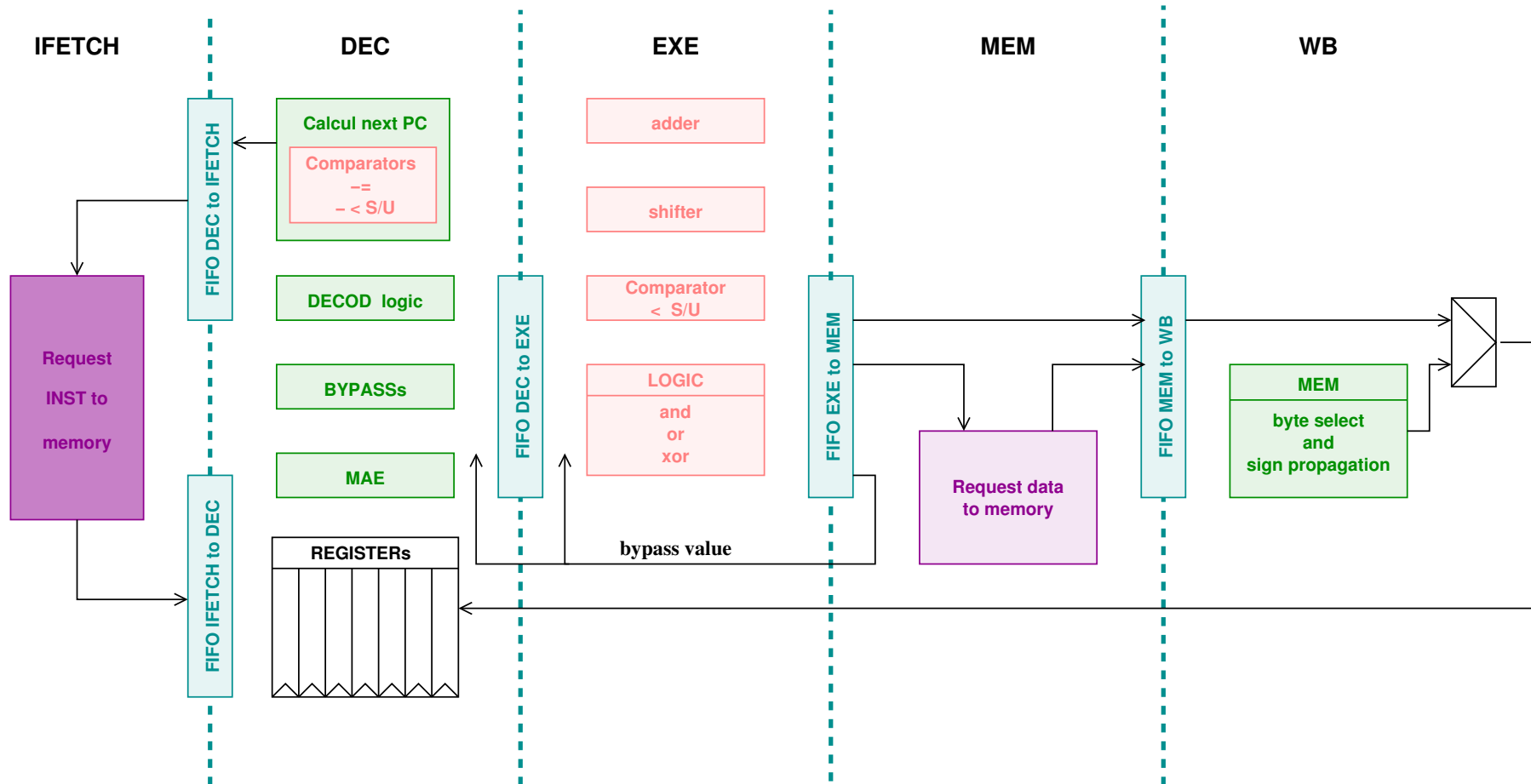
Implemented RISC-V ISA



- RV32I user-space ISA only.
- Target node will be AMS 350nm, 4 metal layers.

- We choose to start with as small possible a component. Always better for debugging...
- Use of a *mature node* so not too expensive and not too much features to implement in the tools.

# Architecture of our RISC-V



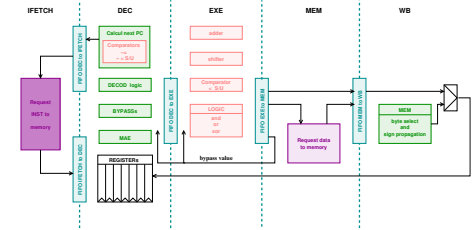
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# RISC-V design using FOSS

└ A First Try at RISC-V

└ Architecture of our RISC-V

Architecture of our RISC-V



- A simple five stage pipeline.
- Based on our experience over the design of the MIPS R3000.
- I'm not the architect, so I couldn't answer tricky design questions...



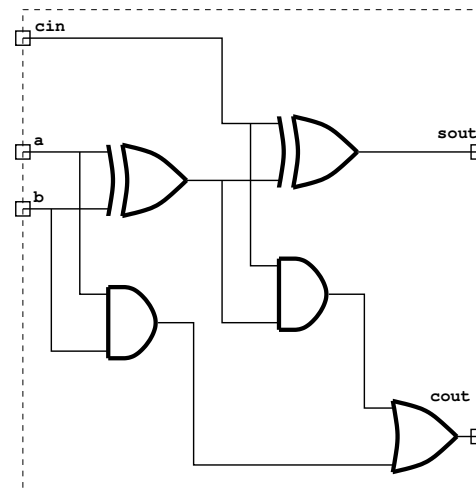
# What Do We Want to Do ?

```
ENTITY halfadder IS
PORT (
  a    : in  BIT;
  b    : in  BIT;
  cout : out BIT;
  sout : out BIT;
);
END halfadder_x2;

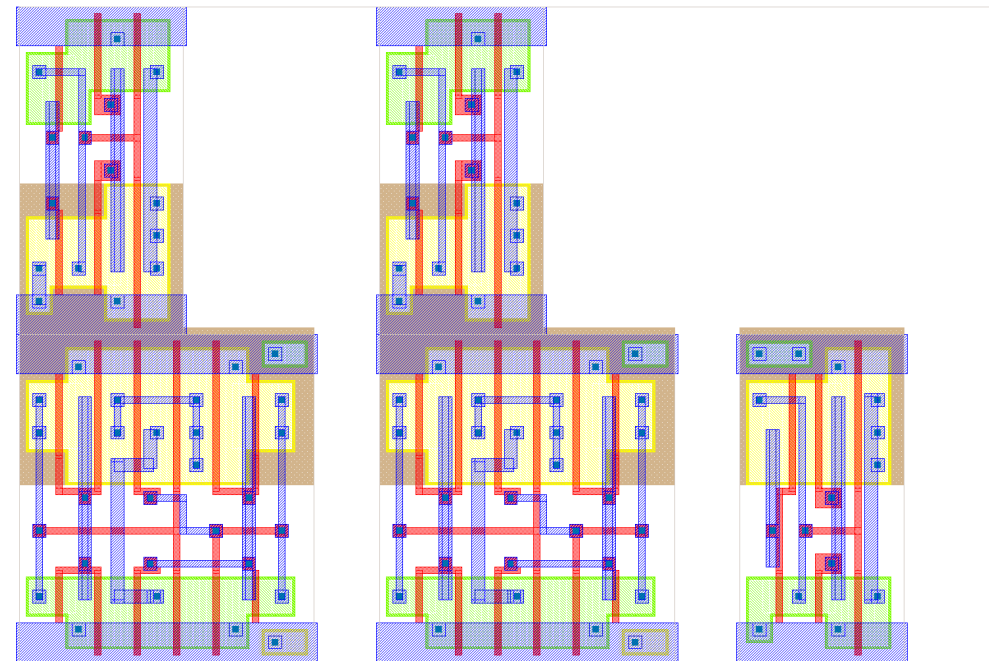
ARCHITECTURE behaviour OF
halfadder IS

BEGIN
  sout <= (a xor b);
  cout <= (a and b);
END;
```

RTL



netlist



layout

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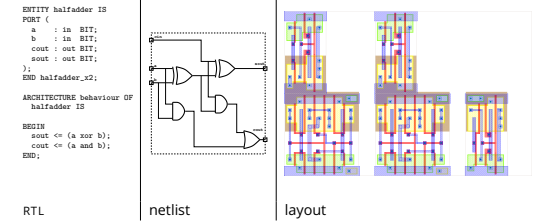
# RISC-V design using FOSS

## └ Design Flow

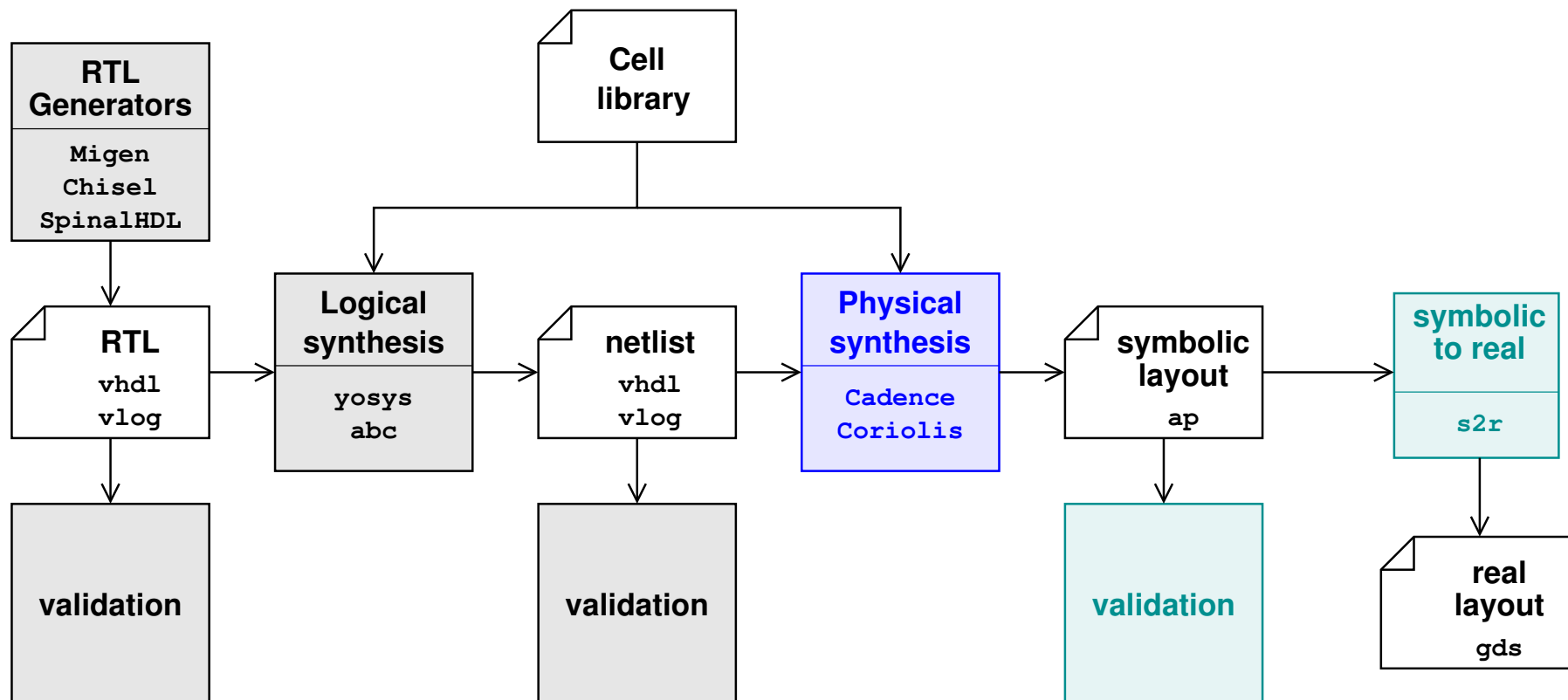
## └ What Do We Want to Do ?

- RTL toward netlist is «logical synthesis».
- netlist toward layout is «physical synthesis».

What Do We Want to Do ?



# General Outline of a VLSI Design Flow



Chisel

<https://www.chisel-lang.org/>

SpinalRTL

<https://github.com/SpinalHDL/>

Migen

<https://m-labs.hk/gateway/migen/>

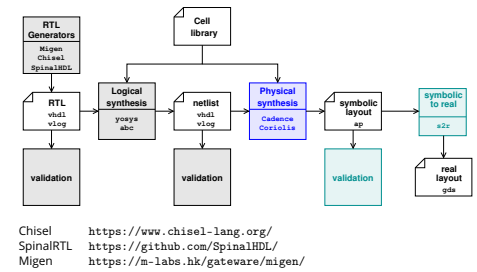
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# RISC-V design using FOSS

## Design Flow

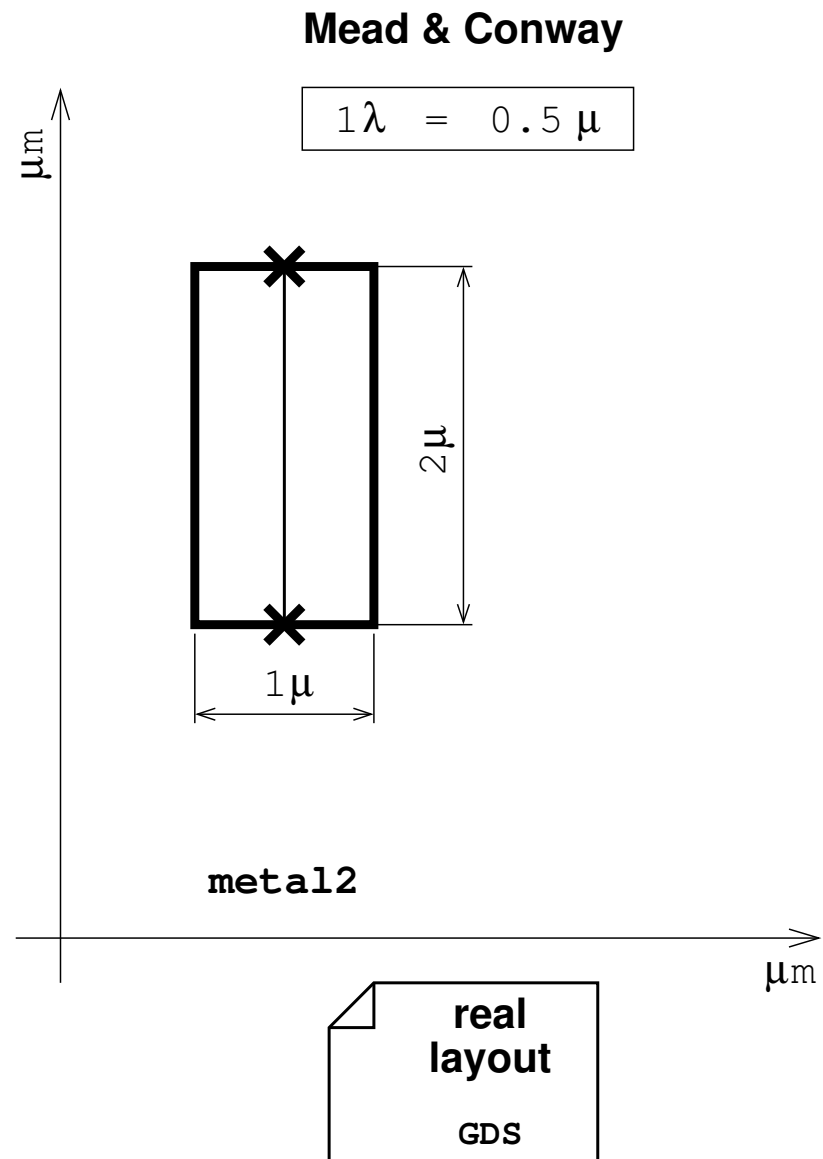
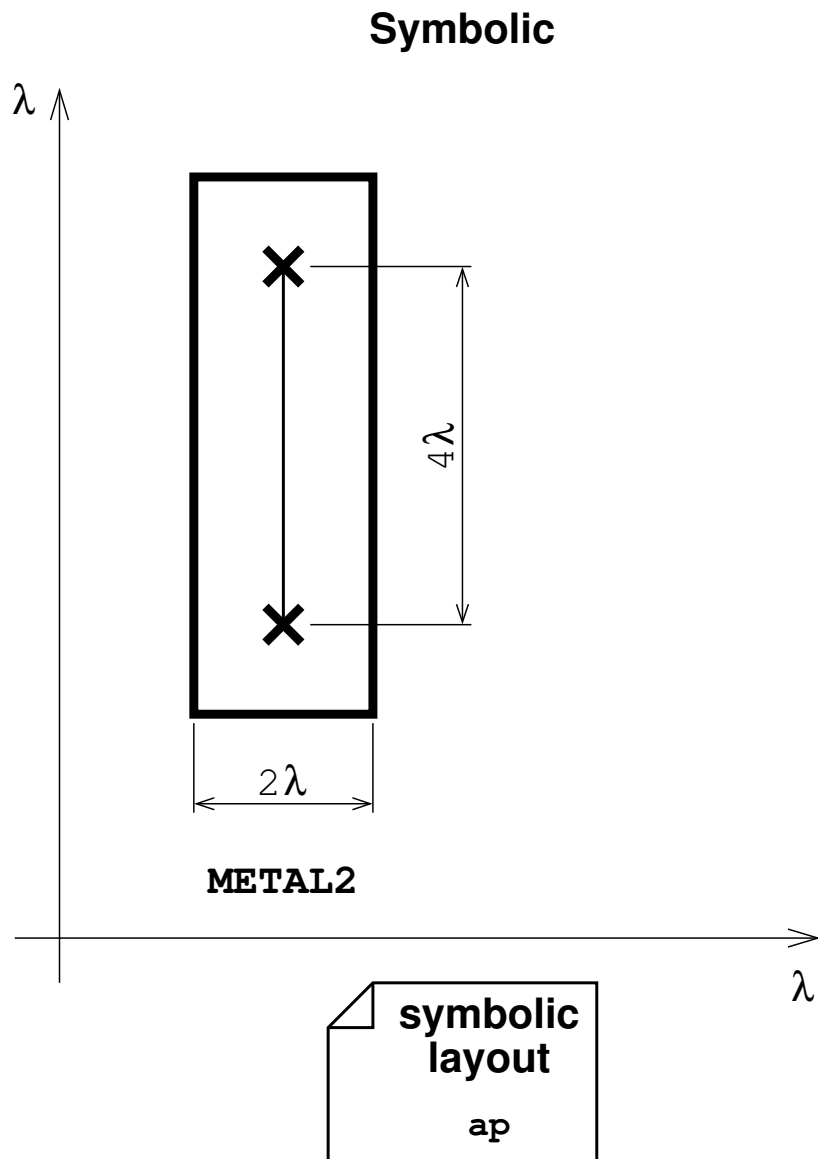
## General Outline of a VLSI Design Flow

General Outline of a VLSI Design Flow



- A word about HDL languages, for now we did it the old way in VHDL. CHISEL and SPINALHDL have a logic more suited for programmers than computer scientists or electronic people. MIGEN is better and written in Python but do not generate VHDL (yet ?). All of them are difficult to extend if an unsupported feature occurs.
- The LIP6 contribution to the flow is mostly focused on the physical design stage.
- More tools exist for the stage before because they can also target FPGAs.
- The equal size of the boxes does not reflect on the hardness of each stage...
- The last step, with s2R will be explained shortly thereafter.

# A brief history of *symbolic layout* (1/2)



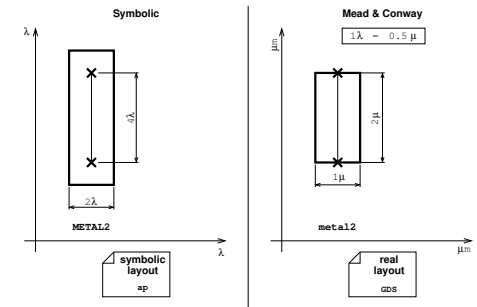
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## RISC-V design using FOSS

### └ Introduction to Symbolic Layout

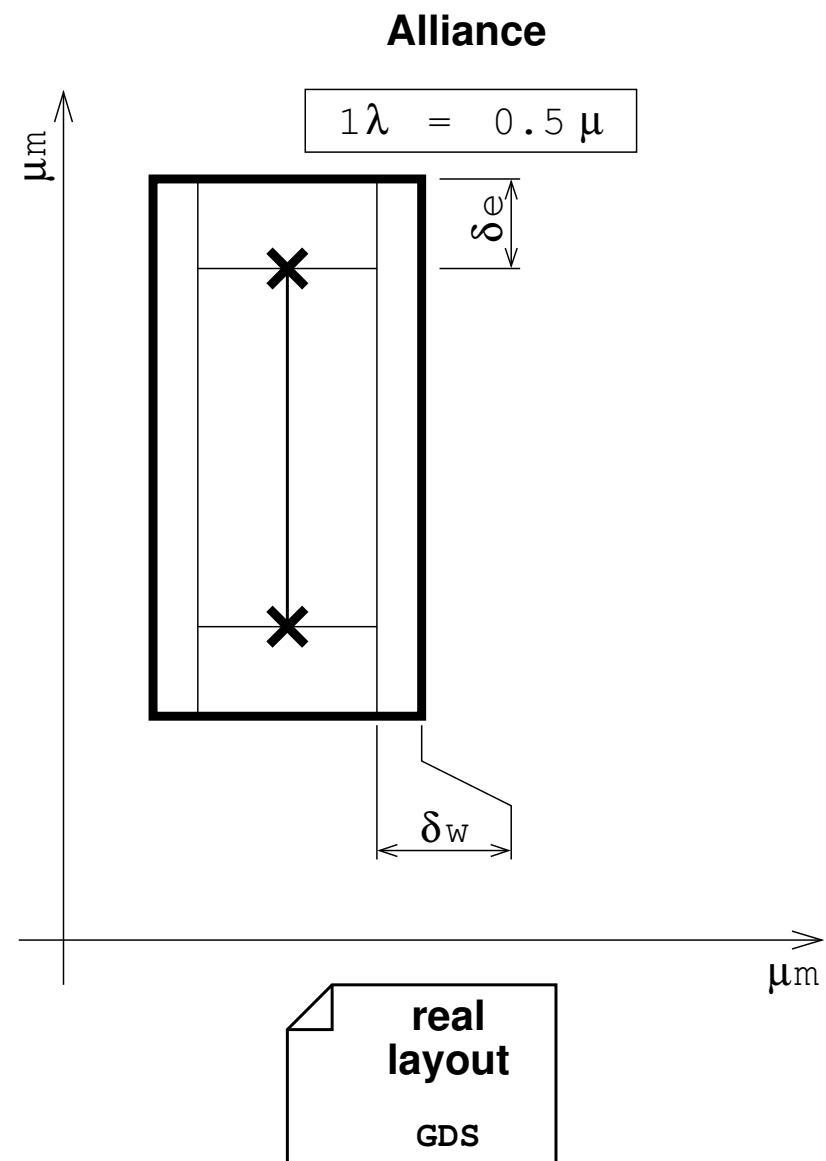
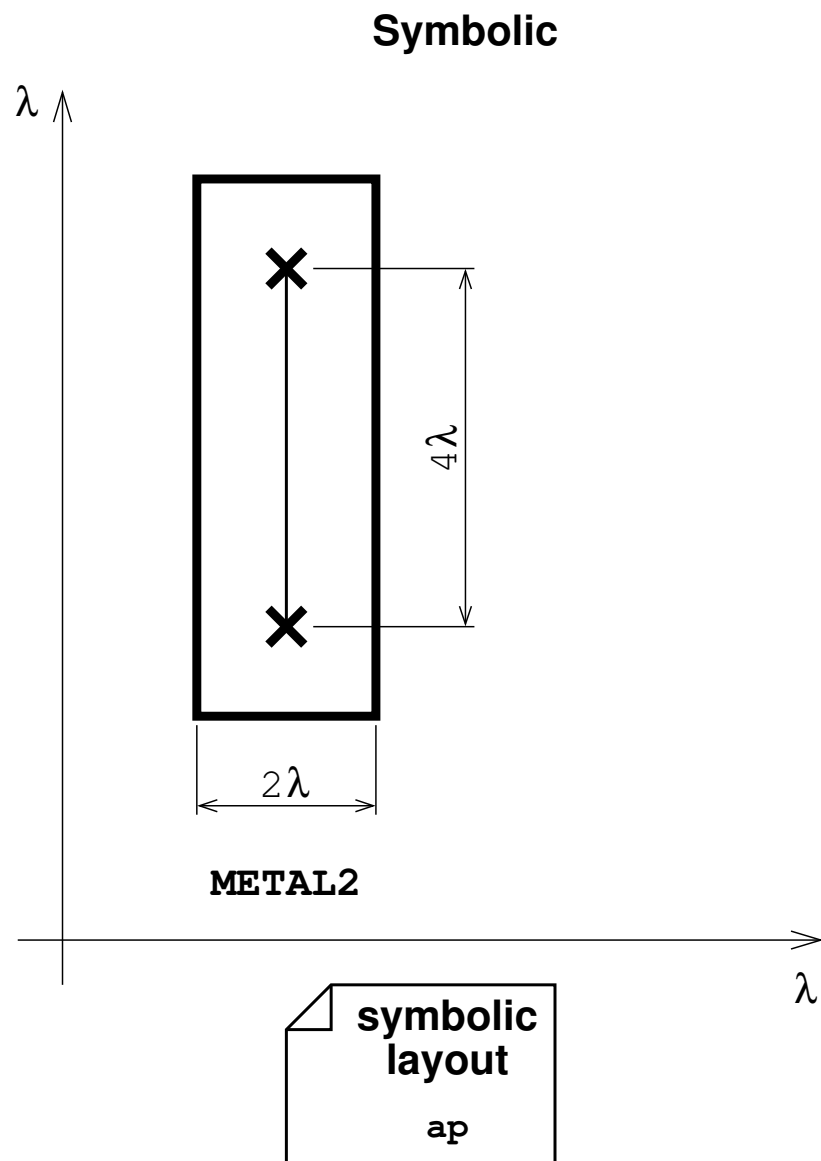
### └ A brief history of *symbolic layout* (1/2)

A brief history of *symbolic layout* (1/2)



- Invented in 1980 by MEAD & CONWAY. Draw your layout using a special dimension unit, the  $\lambda$ . Then scale to the target node. Assume that the shrink rate is almost the same for all layers.
- Designed to cross the boundaries of foundries and nodes.
- Allows a drastic reduction in the number of design rules.
- Main drawback : the area loss, about 10%.
- At the origin of MOSIS.
- Simple shrink finally proven a little bit too rigid.

# A brief history of *symbolic layout* (2/2)



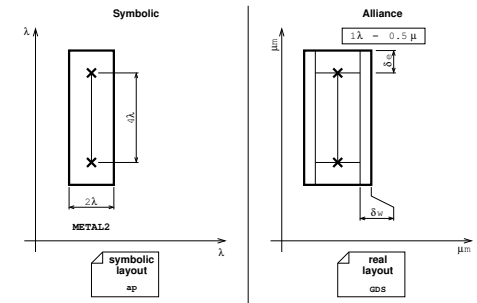
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## RISC-V design using FOSS

### └ Introduction to Symbolic Layout

### └ A brief history of *symbolic layout* (2/2)

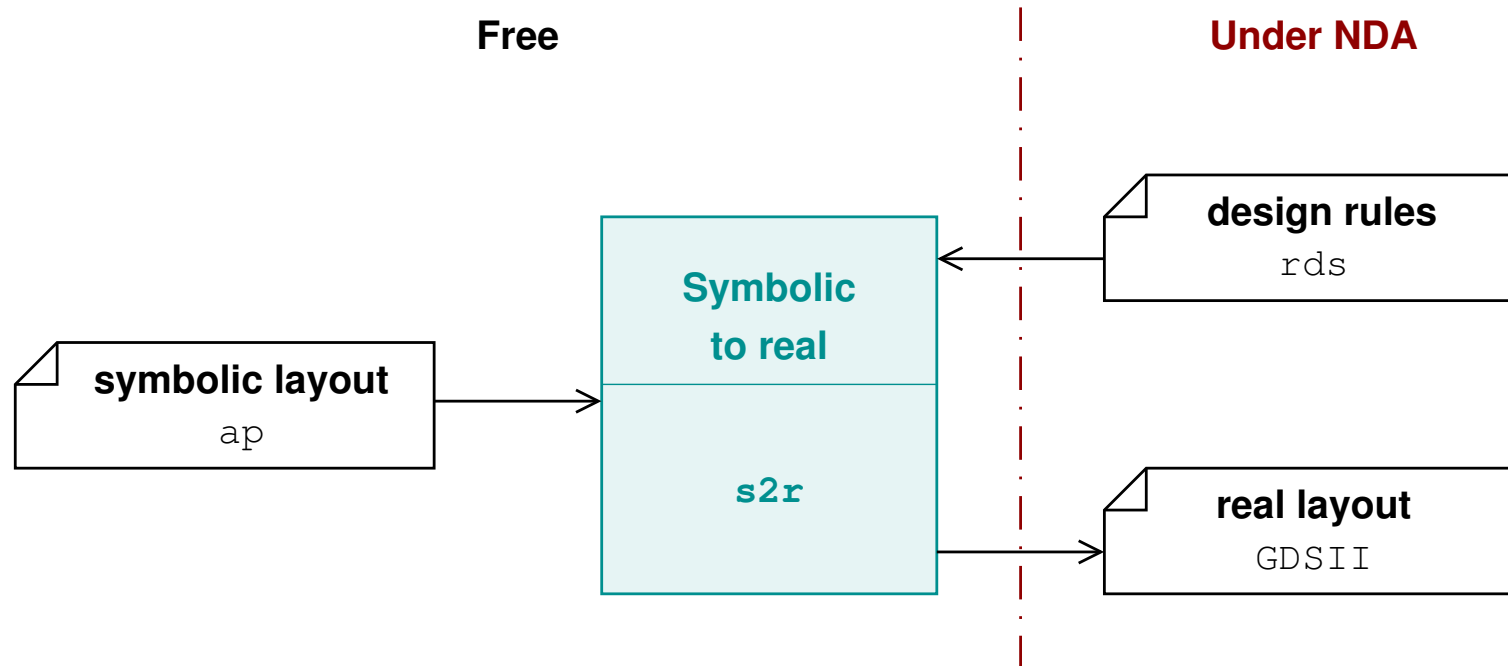
A brief history of *symbolic layout* (2/2)



- Refined by BULL, to give ALLIANCE symbolic. Add cap and width extensions to give more slack in the transformation process.
- BULL is fabless and did not want to be tied to one foundry but didn't want to develop twice it's designs.
- Has a big advantage unforeseen at the time, it is NDA free but still very close the the real layout.
- So, layout **is publishable** and can be **verified** against what comes back from the foundry. Can be critical for security.



# symbolic vs. real layout



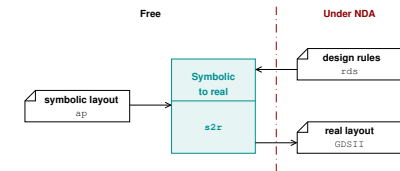
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## RISC-V design using FOSS

### └ Introduction to Symbolic Layout

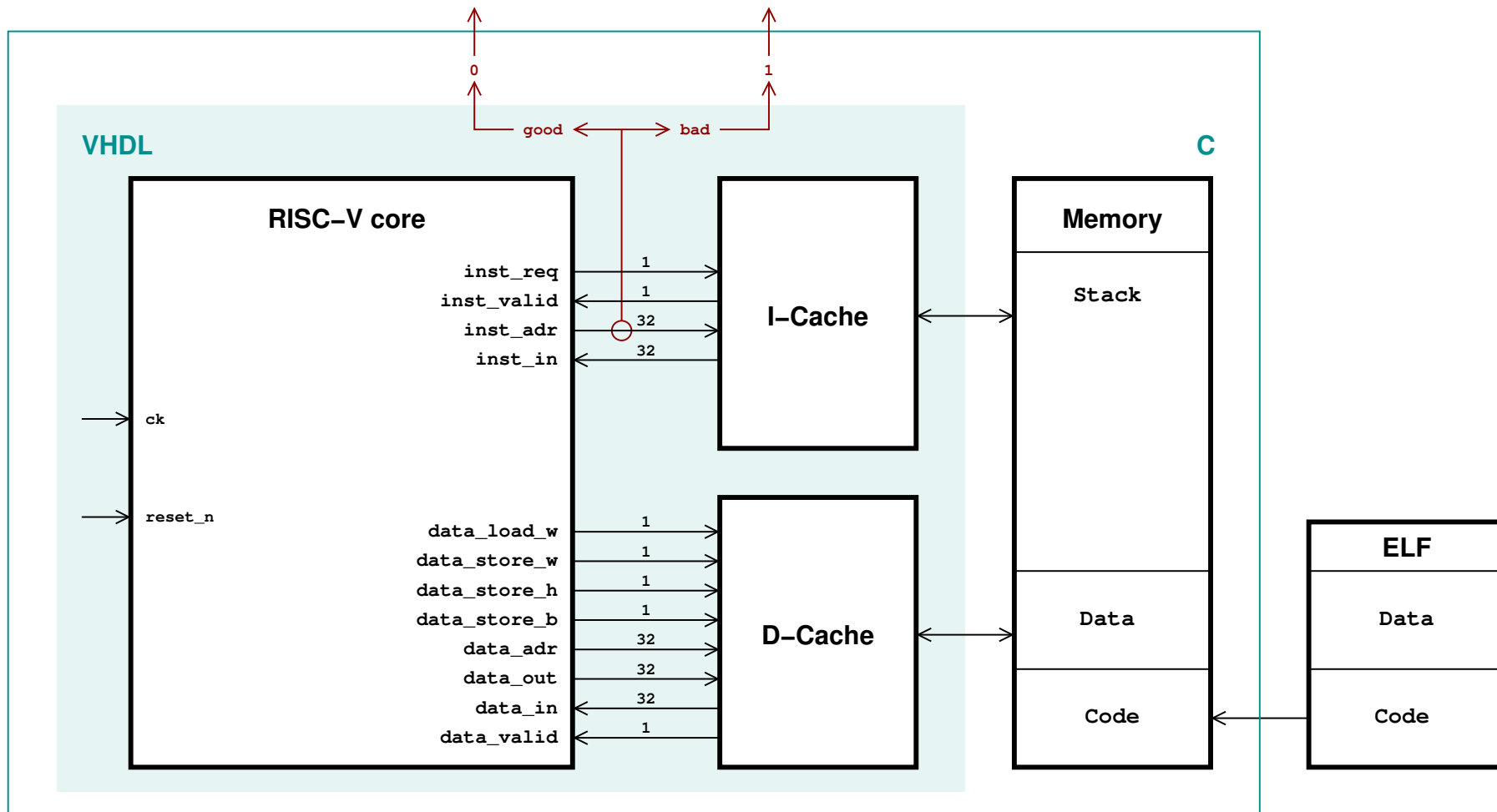
### └ *symbolic vs. real layout*

*symbolic vs. real layout*



- The translation from symbolic to real layout is ensured by the s2R program. It needs a parametrisation for the target node.
- We are working for a way to provide this file (and some more) to other users through the MYCMP service.
- We keep as much as possible of the toolchain on the «left side»...
- This is more difficult when it comes down to timing informations and extraction.
- The other way around NDA has been taken by FREEPDK, which develop fake but realistic design kits. Still they are made mainly for commercial tools.

# Simulation Platform with GHDL



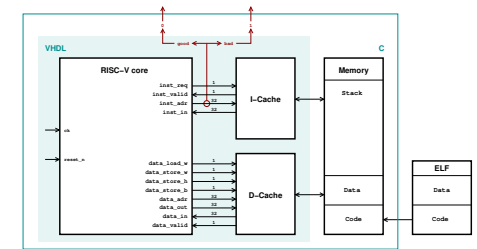
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## RISC-V design using FOSS

└ Description of the Design Flow

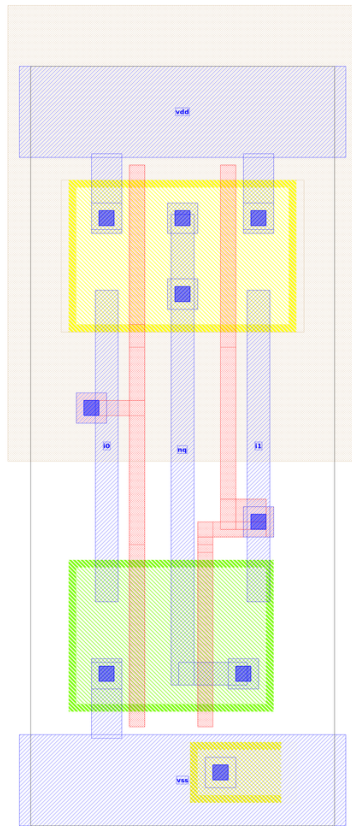
└ Simulation Platform with GHDL

Simulation Platform with GHDL



- We provide the RISC-V VHDL model with a simple access to data and instructions. D-Cache and I-Cache are a misnomer, they are just VHDL proxies for code and data stored in the C part of the platform.
- Code and data are loaded at runtime from an ELF file generated from the tests provided by the RISC-V foundation.
- The whole platform is compiled (both VHDL and C) as a binary.
- It is also used to validate the description after synthesis and place and route.

# The NSXLIB Standart Cell Library



- Portage by N. SHIMIZU from SXLIB.
- Contains 89 cells. Logic gates, D flip-flop, multiplexers.
- Well validated, designs have already been done with it.

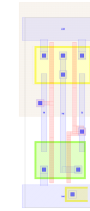
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## RISC-V design using FOSS

### └ Description of the Design Flow

### └ The NSXLIB Standart Cell Library

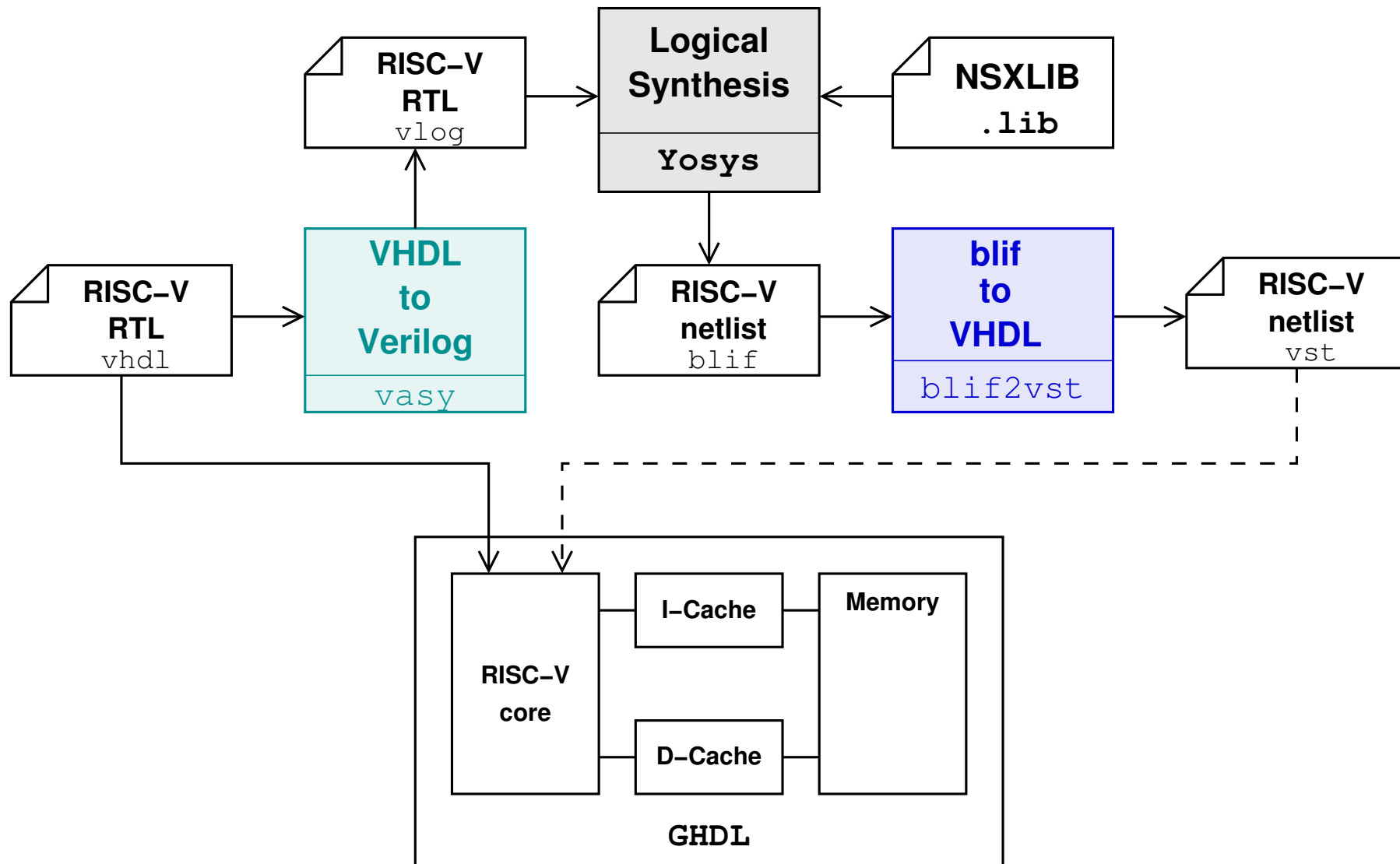
The NSXLIB Standart Cell Library



- Portage by N. SHIMIZU from sXLIB.
- Contains 89 cells. Logic gates, D flip-flop, multiplexers.
- Well validated, designs have already been done with it.

- The symbolic rules needed to be adapted to better fit the deep submicron technologies (45nm and below).
- Automatic characterization procedure with a fake technology to generate a liberty file `.lib` (SYNOPTIS).

# Logical Synthesis



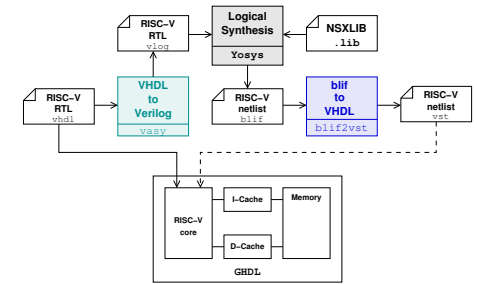
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# RISC-V design using FOSS

## Description of the Design Flow

## Logical Synthesis

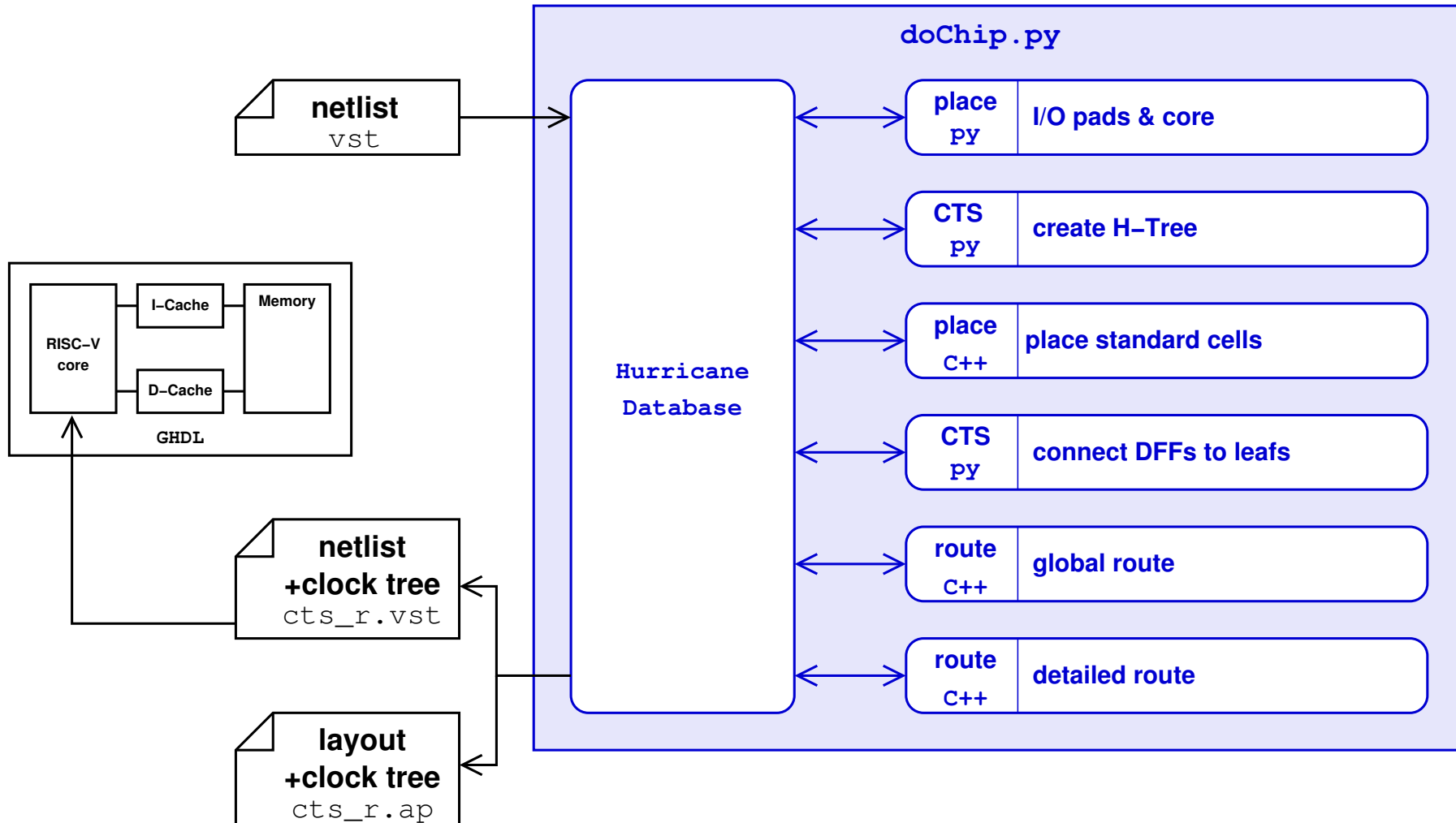
### Logical Synthesis



- We use Yosys to perform the logical synthesis.
- This is a nightmare of format translation between, VHDL, Verilog, blif and vst... (give some details about those formats).
- Color code: **cian** for ALLIANCE, **blue** for CORIOLIS.
- The GHDL platform is used to check that the generated netlist (RTL) is consistent with the behavioral description.



# Physical Synthesis

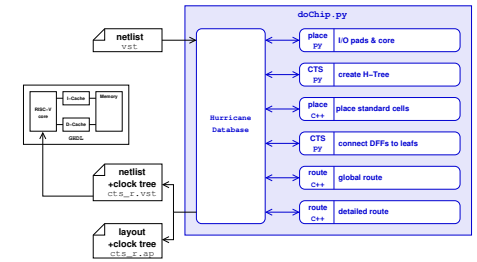


## RISC-V design using FOSS

## └ Description of the Design Flow

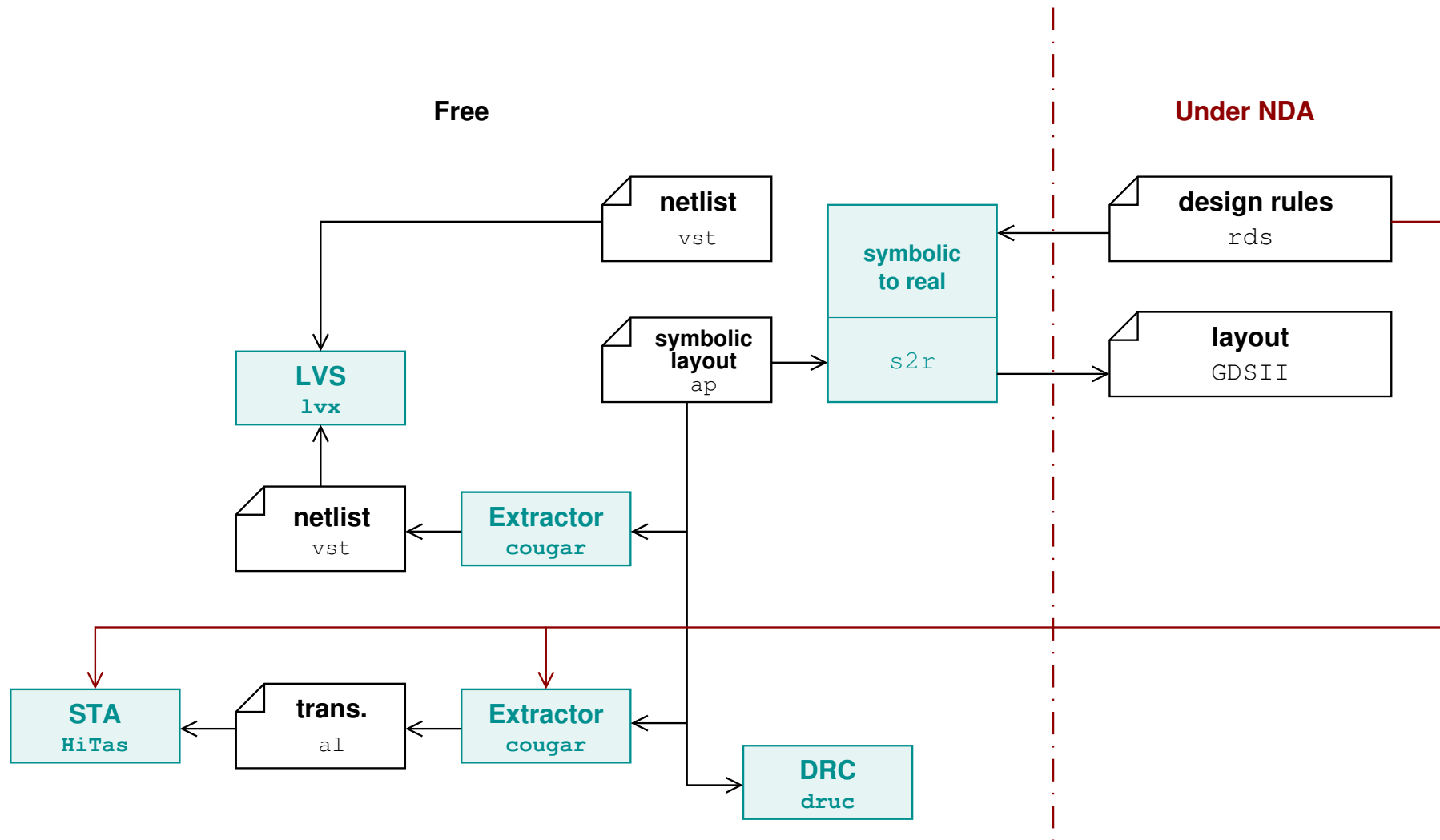
## └ Physical Synthesis

## Physical Synthesis



- Scan-path is inserted in the netlist just after the logical synthesis. It chains the FIFOs, the DECOD & and IFECTH state. Not the register file.
- All tools works *in memory* using the HURRICANE database, this allow a tight integration between the tools. In particular, notice the interleaving between CTS and standard cell placement, this way we can easily connect the DFFs to the nearest clock-tree leaf.
- Another feature of importance is seamless integration between Python and C++ parts. Here again, we can mix them almost any way we want.
- This is so true that there isn't event a CORIOLIS binary. It is only Python scripts that we can tailor to whatever we want.
- As we modify the netlist when inserting the clock tree, we check again with the GHDL platform.
- The placer is analytical, based on SIMPL.

# Validation



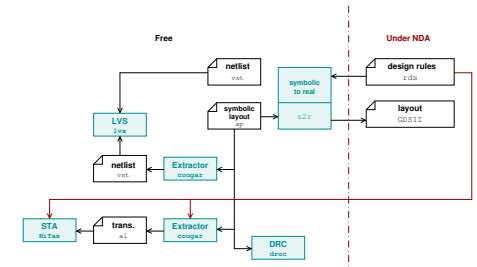
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# RISC-V design using FOSS

## Description of the Design Flow

## Validation

Validation



- The STA HiTas is an old but industry proven tool.
- For the cougar extractor to work it needs technological informations. We supply a fake technology.

# Design Flow Automation

- Alliance Check Toolkit provides a set of GNU Makefiles to fully automate the flow.
- Only one top level Makefile is needed to build a design.
- A regression suite for the tools.
- Various example designs of blocks or whole chips.

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## RISC-V design using FOSS

└─ Description of the Design Flow

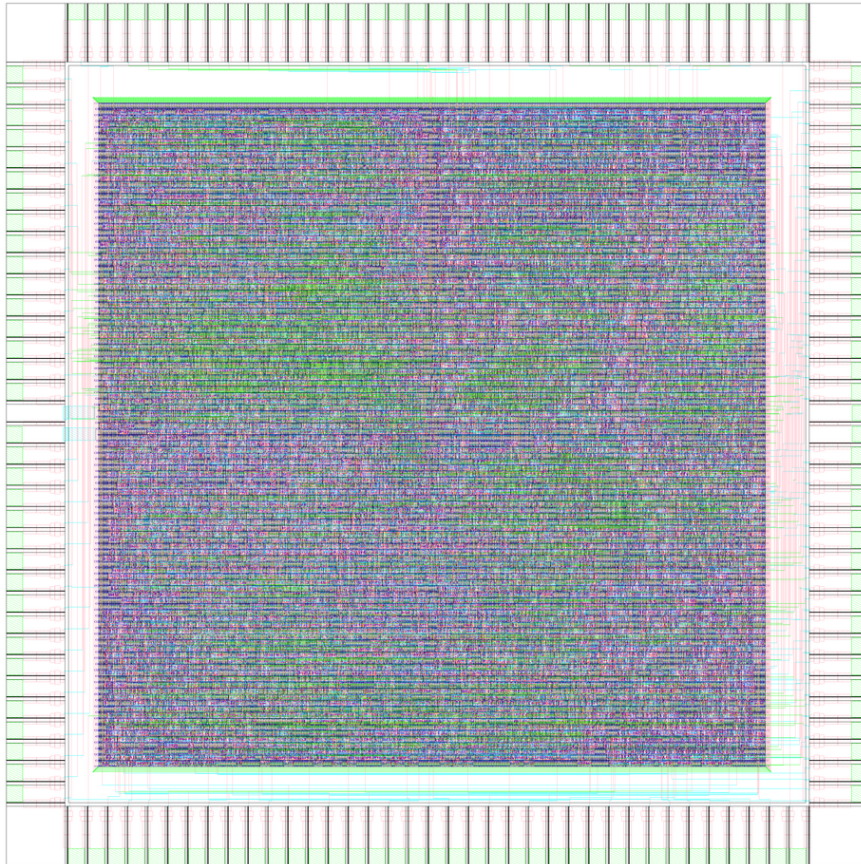
└─ Design Flow Automation

### Design Flow Automation

- ⇒ Alliance Check Toolkit provides a set of GNU `Makefiles` to fully automate the flow.
- ⇒ Only one top level `Makefile` is needed to build a design.
- ⇒ A regression suite for the tools.
- ⇒ Various example designs of blocks or whole chips.

- Alliance Check Toolkit contains a lot of paraphernalia.
- We are at the limit to what can be done with even evolved GNU `Makefiles`. In the future we may write an integrated Python script.

# The Chip



- 11K gates (symbolic layout).
- 144 I/O pad (real layout).
- Chip is core limited.
- Size is  $5 \times 5$  mm ( $25\text{mm}^2$ )

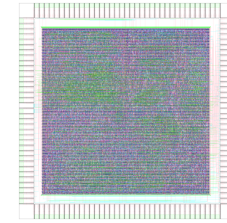
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## RISC-V design using FOSS

### └ Description of the Design Flow

### └ The Chip

The Chip



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- 144 I/O pad (real layout).
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- Size is  $5 \times 5$  mm ( $25\text{mm}^2$ )

- Precisely 11348 gates with Yosys 0.7.
- As we are not finished yet, those results will slightly evolve still.
- The core is symbolic but we use the I/O pad supplied by AMS. This is a part that we cannot make symbolic due to foundry constraints.



# Features Checklist

Implemented :

- Basic scan-path (CORIOLIS).
- Clock-tree (H-Tree).

To be implemented (december 2019):

- Smart scan-path (post-placement path optimization).
- Improve power plan to control IR-drop.
- Check for hold-violations.
- Net high fanout synthesis (HFS).

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## RISC-V design using FOSS

└ Description of the Design Flow

└ Features Checklist

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#### Implemented :

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#### To be implemented (december 2019):

- Smart scan-path (post-placement path optimization).
- Improve power plan to control IR-drop.
- Check for hold-violations.
- Net high fanout synthesis (HFS).

- Of courses, we are talking about features besides classic place and route.
- Our middle term goal is to implement features allowing us to use smaller and smaller nodes.

## References (1/2)

- **GHDL**, Tristan GRINGOLD, <http://ghdl.free.fr/>.
- **Yosys**, Clifford WOLF, <http://www.clifford.at/yosys/>.
- **ALLIANCE**, SU-LIP6  
<http://www-soc.lip6.fr/git/alliance.git/>.
- **CORIOLIS**, SU-LIP6  
<http://www-soc.lip6.fr/git/coriolis.git/>.
- **Alliance Check Toolkit**, SU-LIP6  
<http://www-soc.lip6.fr/git/alliance-check-toolkit.git/>  
Provide the NSXLIB symbolic standard cells library.
- **RISC-V RV32I**, SU-LIP6,  
<http://www-soc.lip6.fr/git/RISC-V.git/>

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# RISC-V design using FOSS

└ Description of the Design Flow

└ References (1/2)

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- **GHD**, Tristan GRINGOLD, <http://ghdl.free.fr/>.
- **Yosys**, Clifford WOLF, <http://www.clifford.at/yosys/>.
- **ALLIANCE**, SU-LIP6  
<http://www-soc.lip6.fr/git/alliance.git/>.
- **CORLIOLIS**, SU-LIP6  
<http://www-soc.lip6.fr/git/coriolis.git/>.
- **Alliance Check Toolkit**, SU-LIP6  
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Pas de notes pour ce transparent.

## References (2/2)

- ISCAS : N. Shimizu, J. Akita, M.-M. Louërat, Haralampos-G. Stratigopoulos, J.-P. Chaput, D. Galayko : “Open Source Hardware and EDA Tools for Analog/Mixed-Signal Design and Prototyping”, 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, (IEEE) (2018)
- FSiC : The development of the NSXLIB standard cell scalable library
- ESSCIRC : “A 29 Gops/Watt 3D-ready 16-core computing fabric with scalable cache coherent architecture using distributed L2 and adaptive L3 caches” E. Guthmuller, C. Fuguet, P. Vivet, C. Bernard, I. Miro-Panades, J. Durupt, E. Beigne, D. Lattard, S. Cheramy, A. Greiner, Q. Meunier and P. Bazargan Sabet

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# RISC-V design using FOSS

└ Description of the Design Flow

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- FSIC : The development of the NSXLIB standard cell scalable library
- ESSCIRC : "A 29 Gops/Watt 3D-ready 16-core computing fabric with scalable cache coherent architecture using distributed L2 and adaptive L3 caches" E. Guthmuller, C. Fuguet, P. Vivet, C. Bernard, I. Miro-Panades, J. Durupt, E. Beigne, D. Lattard, S. Cheramy, A. Greiner, Q. Meunier and P. Bazargan Sabet

Pas de notes pour ce transparent.

And now, let's have a demo...

## RISC-V design using FOSS

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└ Demo

└ And now, let's have a demo...

- Run the logical synthesis stage on the console, then switch to graphical mode for the physical synthesis.
- Commands:

```
ego@home:RISC-V> cd PlaceAndRoute
ego@home:PlaceAndRoute> make scan
ego@home:PlaceAndRoute> cgt -V -cell=riscv_core_scan
```

Generate the chip from the pads using AMS pads.  
Place chip (with clock tree).  
Do not forget to go down the corona.  
Global then detail route the corona / core.
- Comment on Etesian analytical placer (force directed).