Development of a RV64GC IP core for the GRLIB IP Library

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Introduction

Cobham Gaisler AB

Since 2 December 2014

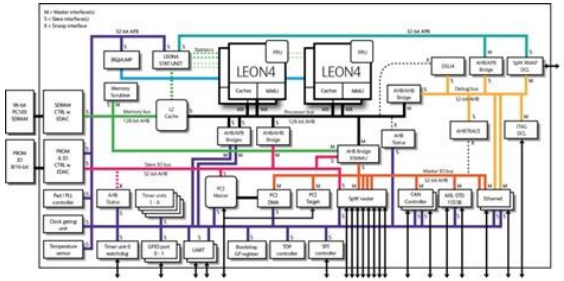
- **Cobham Gaisler** is a world leader in processors for space applications like satellites & launchers
- Located in Gothenburg, Sweden
- Established in 2001 and acquired by Aeroflex in 2008
- Fully owned subsidiary of Cobham plc since 2014
- Management team with >100 years combined experience in the space sector:
- 34 employees with expertise within electronics, ASIC and software design
- Complete facilities in-house for ASIC and FPGA design

To provide processors that enable new scientific missions, and allow new ways to utilize space constellations for commercial use.

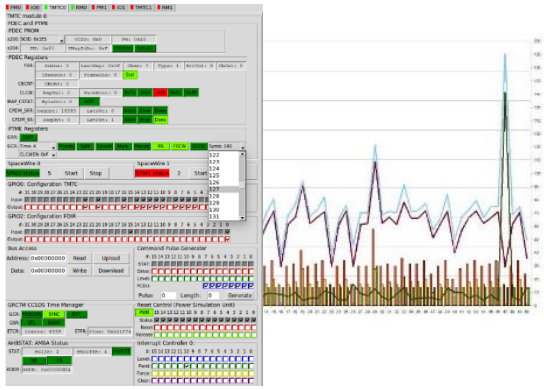
Cobham Gaisler Processor Solutions

One-Stop-Shop

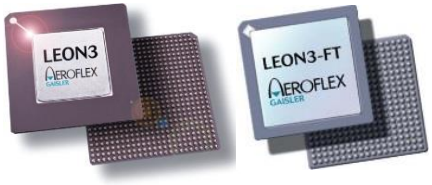
Synthesizable IP Core Library

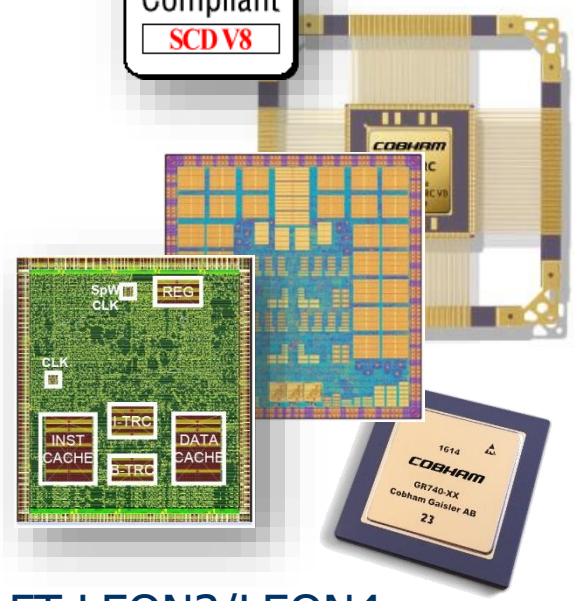


Simulators, Debuggers, Operating Systems, Compilers



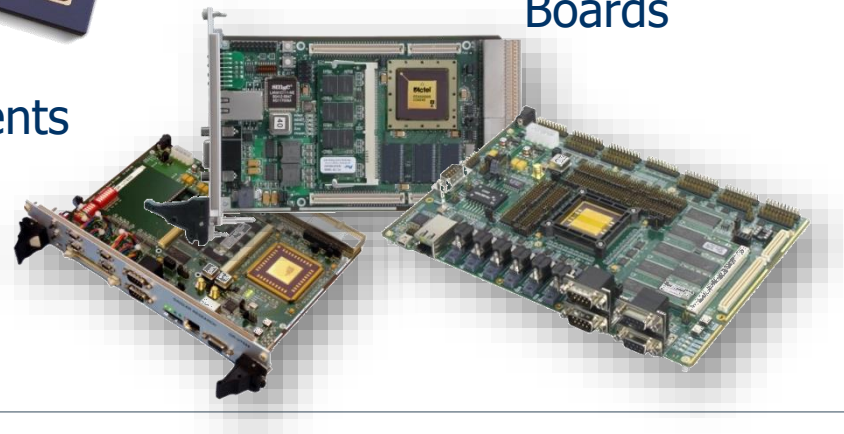
FT FPGA Processors





FT LEON3/LEON4 Processor Components

Development Boards



System Testbeds

RISC-V Contribution

Cobham is now a Multi-Architectural Company

Cobham continues to be committed to and invested in the SPARC architecture and its LEON implementations.

SPARC/LEON will be maintained and further developed going forward. The company has customers expecting it to provide components and support for decades to come. This is also ensured via long term supply agreements.

The RISC-V architecture is expected to grow in the future with a larger number of developers compared to SPARC V8.

Going forward, Cobham will add RISC-V to its product portfolio as a complement to SPARC not as a replacement.

Cobham RISC-V solution

- Cobham has 15+ years experience designing open hardware
  - First GPL release of LEON+GRLIB in 2002
  - NOEL-V (RISC-V) will be distributed from Q1 2020
- GRLIB-FT IP cores has a solid space flight heritage
  - Extensive know-how of space computing, not only in processors
- Cobham provides a complete solution for custom SOC
  - Implementation in FPGA and ASIC
- Software support and drivers
  - Linux
  - RTEMS
  - VxWorks
  - Bare-metal

Why another RISC-V implementation?

- Cobham is developing its own RISC-V implementation: NOEL-V
  - As opposed to licensing from 3rd party
- Full control of the design means short path to new custom features
  - I.e. not dependent on external IP
- Experienced processor team in-house
- GRLIB based implementation makes use of existing infrastructure
- Allows for flexible license options
  - Flight
  - Commercial
  - Educational
  - Non-paid
  - Cobham branded components

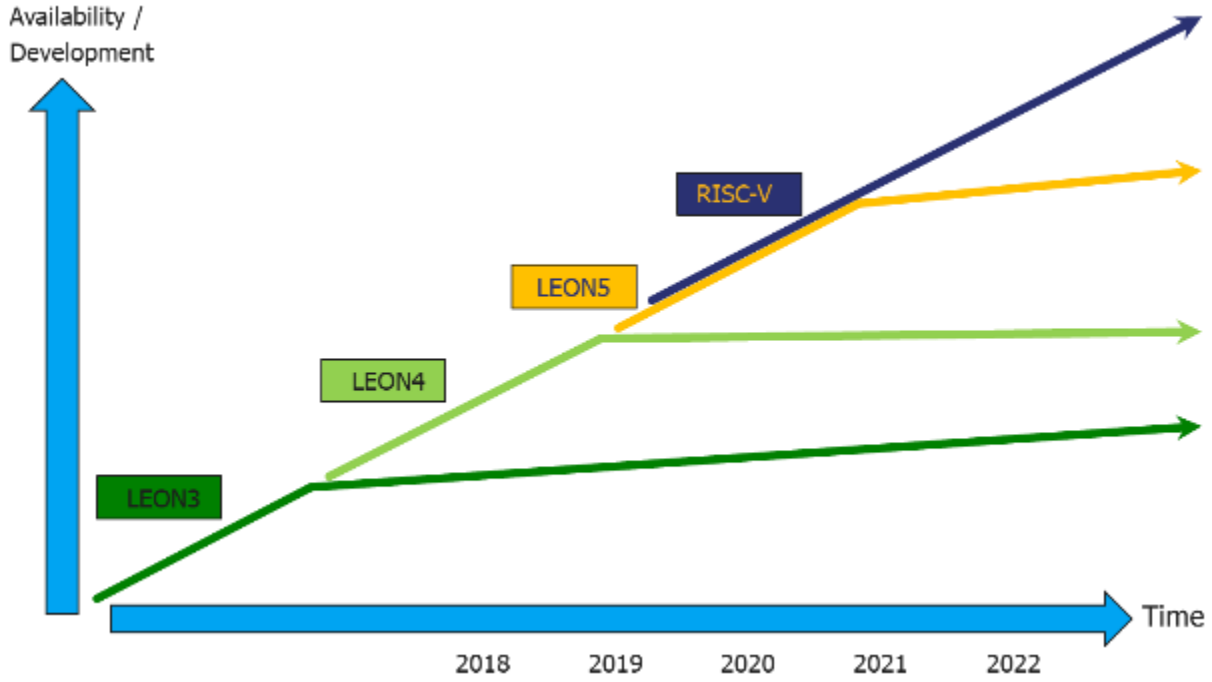
RISC-V contribution

What can Cobham Gaisler contribute to the RISC-V community?

- With NOEL-V we will help bringing space computing to RISC-V
  - ...and bring RISC-V to space
- Make GRLIB IP core library available to the RISC-V platform
  - 100+ production quality IP cores
  - Several available under dual GPL/commercial license
  - Software driver support
  - Portable to FPGA and ASIC
  - Wide support for popular FPGA evaluation boards

Processor Roadmap

SPARC V8 and RISC-V



- Long-term commitments:
  - LEON3 maintained for FPGA architectures
  - LEON5 maintained for high-performance FPGAs and ASICs, legacy users
  - Software support maintained for LEON3, LEON4, LEON5
  - RISC-V developed for modern processing solutions
  - Building new RISC-V engineering group, parallel to existing LEON team

RISC-V Processor Core

Primary goals:

- RISC-V 64-bit compliant processor core
- Superscalar – baseline is dual issue
- Fault Tolerance - Error Correction Codes (ECC)
- Cybersecurity (proprietary solutions)
- Enable ISO 26262/FUSA certification (Road vehicles – Functional safety)
- Leverage foreseen uptake of RISC-V software and tool support in the commercial domain
- Compatible with GRLIB IP Core library

Primary feature set:

- RISC-V RV64GC
- AHB and AXI4 bus support

Supportive activities

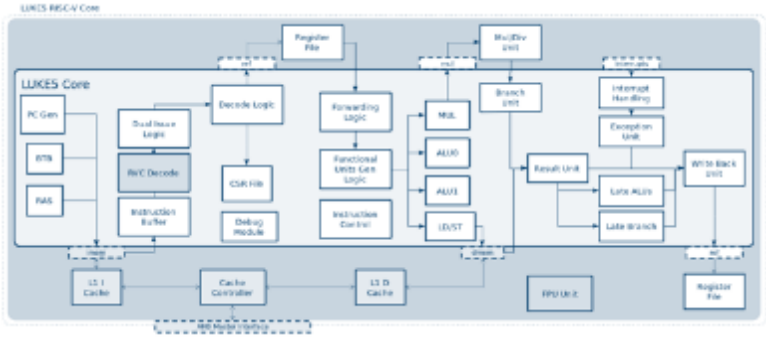
- RISC-V Foundation Membership in 2019

Target technologies:

- ASIC implementations for space applications
- High-end space FPGAs: Kintex Ultrascale

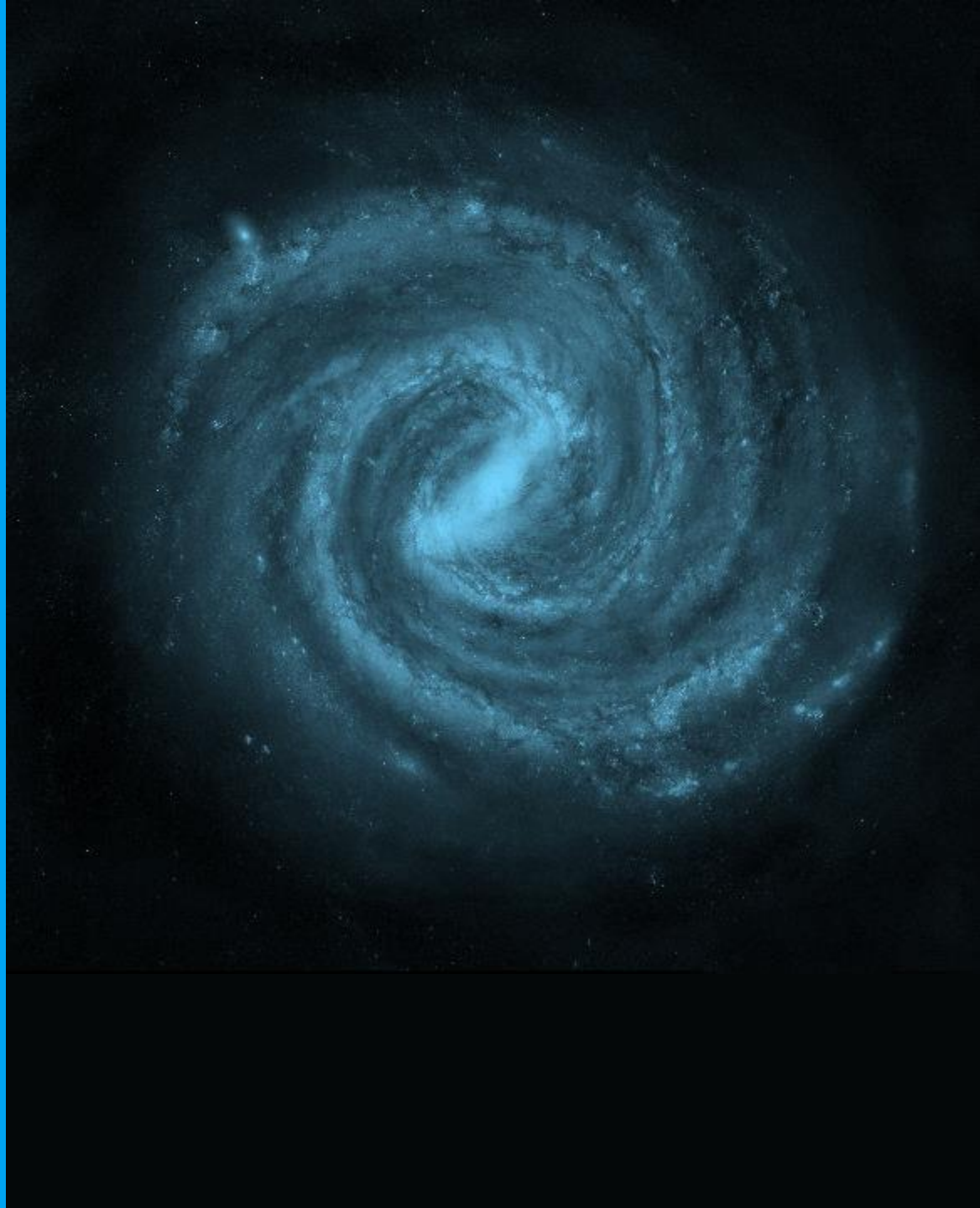
Target applications:

- General purpose payload processing
- Mixed platform and payload applications
- With future DDR4 SDRAM controller, specifically targeted for space applications



Cobham Gaisler GRLIB IP Library©

Software



NOEL-V Software ecosystem

Outlook for NOEL-V

Operating systems

- Bare-metal environment
  - Rich set of peripheral drivers
  - Open-source license
- Linux
  - GRLIB device drivers
  - Open-source license
- VxWorks 7 SMP
- RTEMS-5 SMP
  - GRLIB peripheral drivers at production level already in mainline kernel
  - ESA activity is currently performing space qualification of the mainline kernel
  - Open-source license

Hardware debuggers

- GRMON
  - Tcl scripted command line interface
  - JTAG, Ethernet, USB, UART, SpaceWire
  - GDB connection for C/C++-level debug
  - NOEL-V and LEON based chips
  - Other RISC-V under evaluation

Simulators

- TSIM multiprocessor SOC simulator
  - Currently LEON product
  - RISC-V support under evaluation

Compiler Toolchains

- GCC and LLVM, NOEL-V optimizations

Boot loaders

- Flight quality boot loader will be evaluated
  - Port of existing LEON version

Summary

Summary

- Cobham Gaisler has with LEON utilized the open SPARC standard to become one of the world leaders in space-grade processor solutions.
- We see the rise of RISC-V as a positive movement that is well suited to our business model.
- NOEL-V is Cobham Gaisler's in-house RV64GC implementation that may be used for future processor products and will be released as part of the free open source GRLIB IP library.