Syntacore™
Custom cores and tools

RISC-V

Open-source processor IP in the SCRx family of the RISC-V compatible cores by Syntacore

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2nd RISC-V Meeting, Paris, Oct 2019

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Syntacore introduction

IP company, founding member of RISC-V foundation

Develops and licenses state-of-the-art RISC-V cores

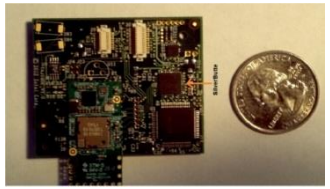
- Silicon-proven and shipping to customers
- 4+ years of *focused* RISC-V development
- Core team comes from 10+ years of highly-relevant background
- SDKs, samples in silicon, full collateral

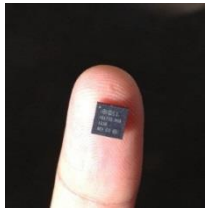
Full service to specialize CPU IP for customer needs

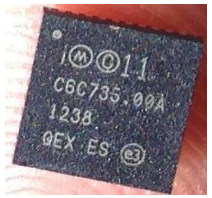
- One-stop workload-specific customization for 10x improvements
  - with tools/compiler support
- IP hardening at the required library node
- SoC integration and SW migration support

Company background

- Est 2015 , 30+ EEs
- HQ at Cyprus (EU)
  - R&D offices in St.Petersburg and Moscow (Russia)
- Representatives in China/APAC, EMEA







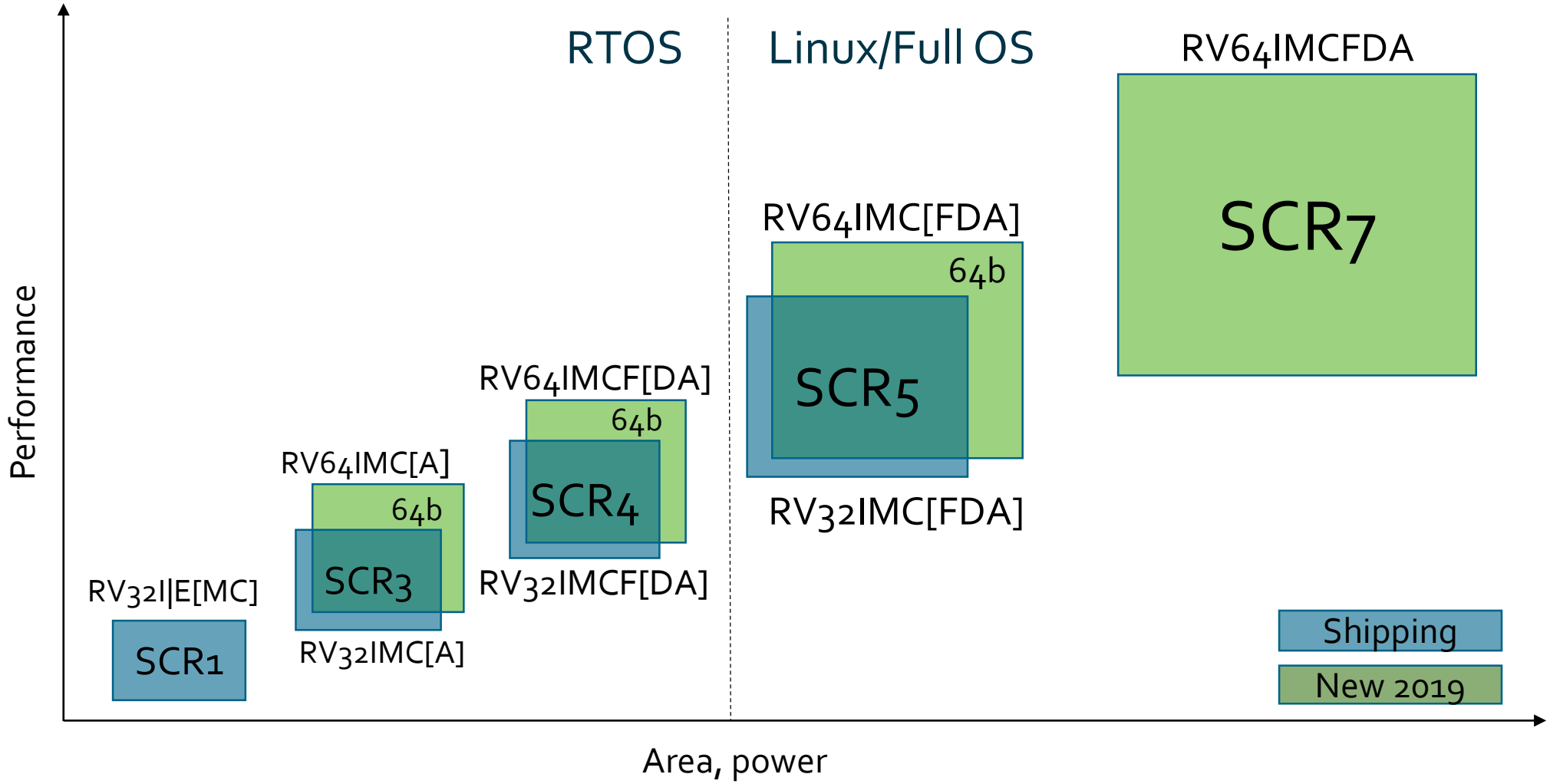
Team background:

- 10+ years in the corporate R&D (major semi MNC)
- Developed cores and SoC are in the mass productions
- 15+ tapeouts, 180..14nm

Expertise:

- Low-power and high-performance embedded cores and IP
- ASIP technologies and reconfigurable architectures
- Architectural exploration & workload characterization
- Compiler technologies

SCRx baseline cores 2019

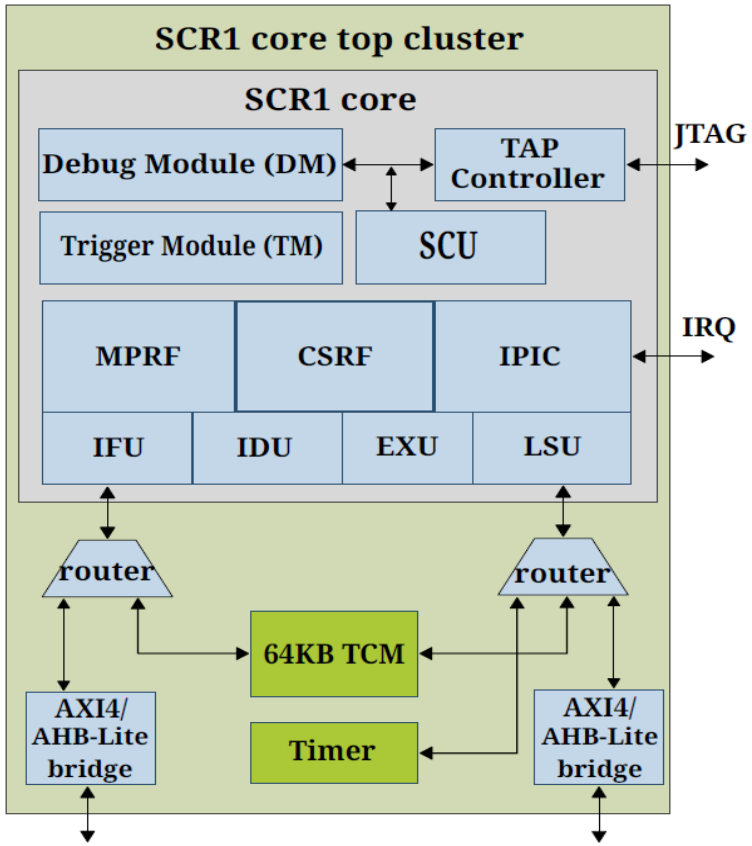


Open-source SCR1 core

Compact MCU core for deeply embedded applications and accelerator control

- **Open sourced under SHL-license** since May 2017
  - Industry-grade with unrestricted commercial use allowed
- RV32I|E[MC] ISA, M-mode only
- **<15 kGates** in basic RV32EC configuration
- Configurable 2 to 4 stages pipeline
- Optional IPIC with 16 IRQs
- Optional RISC-V Debug subsystem with JTAG interface
- Verification suite
- Extensive documentation
- Updated and maintained
  - Best-effort support provided, commercial available

UPD



https://github.com/syntacore/scr1

SCR1 codebase

Codebase:

- SystemVerilog, ~10000 LOC, ~500kB code size
- 33 configurable options
- 3 predefined/recommended configurations:
  - **Minimal** RV32EC w/o uncore
  - **Basic** RV32IC with debug/irq
  - **Max performance** RV32IMC

Configuration	Area, kgates	Artix-7 utilization*, LUT/FF	Coremark**, MHz
Minimal RV32EC w/o uncore	11	2099 / 818	1.01
Basic RV32IC with debug/irq	26	4355 / 2267	1.27
Max performance RV32IMC	33	5753 / 2413	2.95

* utilization for Digilent Arty board (XC7A35T)

** Coremark 1.0, GCC 8.1 BM from TCM, -O3 -funroll-loops -fpeel-loops -fgcse-sm -fgcse-las -flto

SCR1 out-of-box simulation

Quick start from SCR1 repo root:

```
> make run_verilator_wf ARCH=IMC
```

All major simulators supported:

- Altera ModelSim
- Synopsys VCS
- Cadence NCSim
- Verilator + waveforms

Tests:

- RISC-V ISA tests
- RISC-V Compliance suite
- Dhrystone benchmark
- CoreMark benchmark
- Other tests/sample apps

SCRx IP features at glance

Features			RTOS/ Bare Metal			Linux/ "Full" OS	
			SCR1* (FREE!)	SCR3	SCR4	SCR5	SCR7
Width		32bit	●	●	●	●	
		64bit		●	●	●	●
ISA			RV32I[E][MC]	RV[32|64]IMC[A]	RV[32|64]IMCF[AD]	RV[32|64]IMC[AFD]	RV64IMCAFD
Pipeline type			In-order	In-order	In-order	In-order	Superscalar
Pipeline, stages			2-4	3-5	3-5	7-9	10-12
Branch prediction				Static BP, RAS	Static BP, RAS	Static BP, BTB, BHT, RAS	Dynamic BP, BTB, BHT, RAS
Execution priority levels			Machine	User, Machine	User, Machine	User, Supervisor, Machine	User, Supervisor, Machine
Extensibility/customization			●	●	●	●	●
Execution units	MUL/DIV	area-opt	●	○	○		
		hi-perf	○	●	●	●	●
	FPU				●	●	●
Memory subsystem	TCM		○	○	○	○	○
	L1$ w/ECC			○	○	●	●
	L2$ w/ECC					○	○
	MPU			●	●	●	●
	MMU, virtual memory					●	●
Debug	Integrated JTAG debug		●	●	●	●	●
	HW BP		1-2	1-8 adv ctrl	1-8 adv ctrl	1-8 adv ctrl	1-8 adv ctrl
	Performance counters		○	○	○	○	○
Interrupt Controller	IRQs		8-32	8-1024	8-1024	8-1024	8-1024
	Features		basic	advanced	advanced	advanced+	advanced+
SMP support				up to 4 cores with coherency			up to 8-16 cores
I/F options	AHB		●	○	○	○	○
	AXI4		○	●	●	●	●
	ACE						○

* Download SCR1 free at www.github.com/syntacore/scr1

Baseline cores:

- Clean-slate designs in System Verilog
- Configurable and extensible
- 100% compatible with major EDA flows

Fully featured SW development suite

Stable IDE in production:

- GCC 8.1
- GNU Binutils 2.31.0
- Newlib 3.0
- GNU GDB 8.0.50
- Open On-Chip Debugger 0.10.0
- Eclipse 4.9.0

Hosts: Linux, Windows

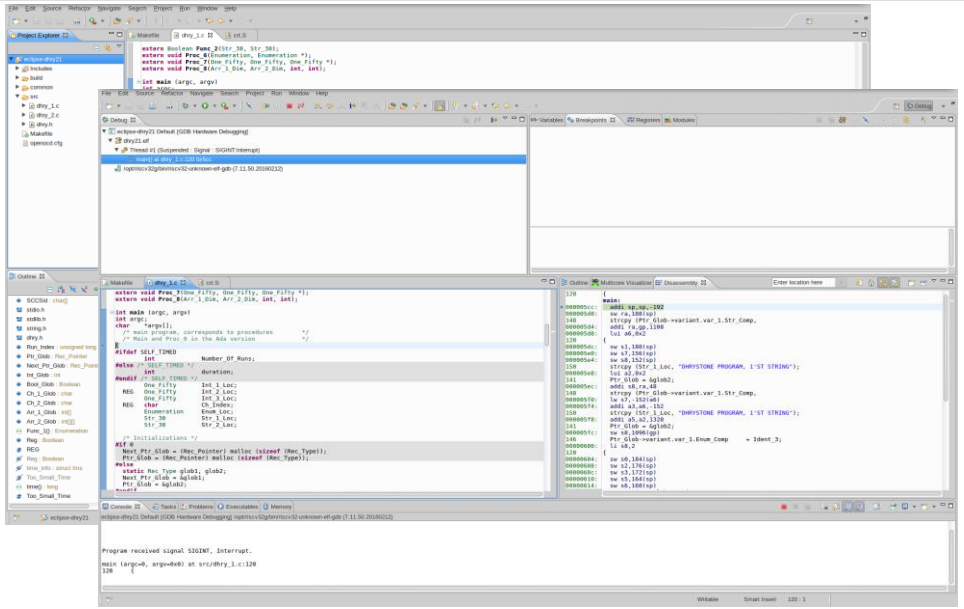
Targets: BM, Linux (beta)

Also available:

- LLVM 5.0
- CompCert 3.1
- 3rd party vendors in 2019

Simulators:

- Qemu
- Spike
- 3rd party vendors



JTAG-based debug solutions:

Supports: Segger J-link, Olimex ARM-USB-OCD family, Digilink JTAG-HS2, Lauterbach trace32, more vendors in 2019

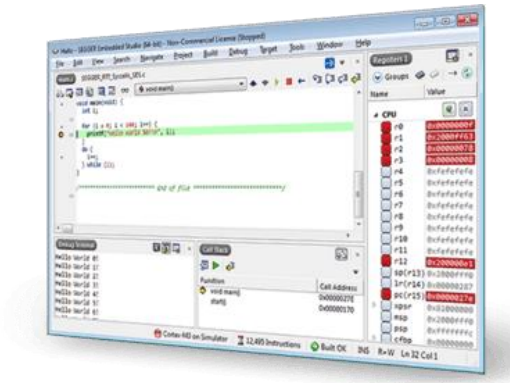
3rd party tools support

- Lauterbach Trace32

https://www.lauterbach.com/frames.html?pro/pro__syntacore.html

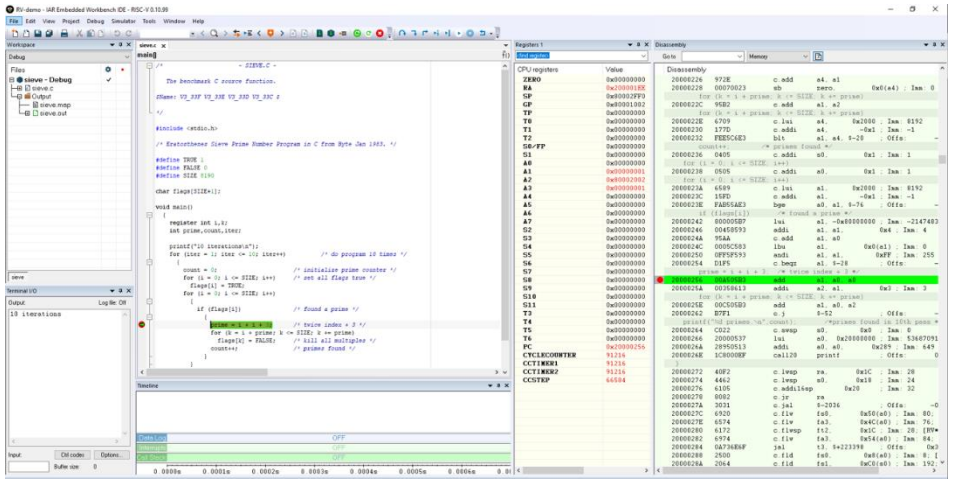
- Segger Embedded Studio

https://wiki.segger.com/Syntacore_SCR1_SDK_Arty



- IAR Embedded Workbench
- NEW!

https://www.iar.com/iar-embedded-workbench/#!?architecture=RISC-V

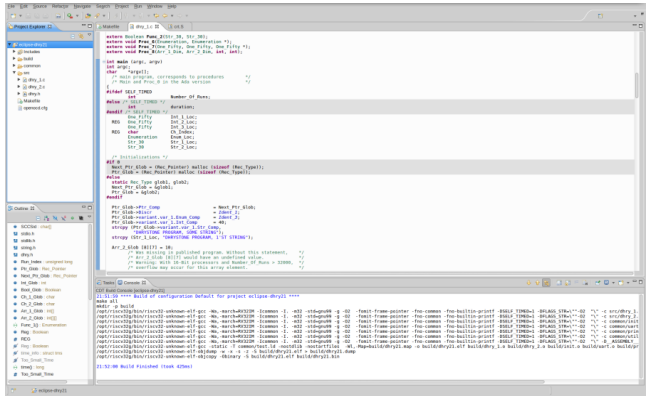


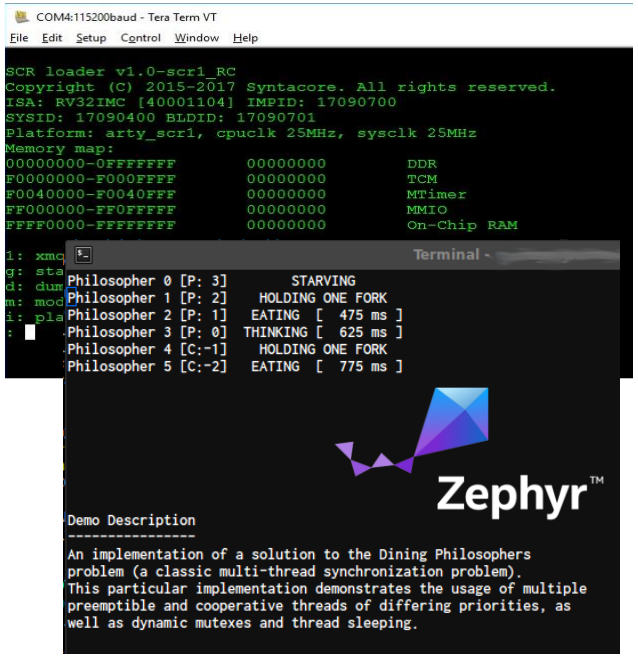
...more in 2019

SCRx SDKs

Stable Eclipse/gcc based toolchain with IDE:

- GCC 8.1
- GNU Binutils 2.31.0
- Newlib 3.0
- GNU GDB 8.0.50
- Open On-Chip Debugger 0.10.0
- Eclipse 4.9.0



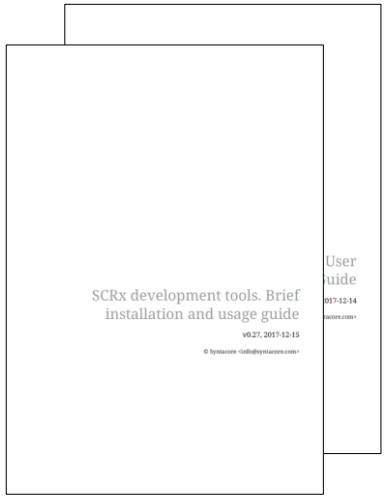


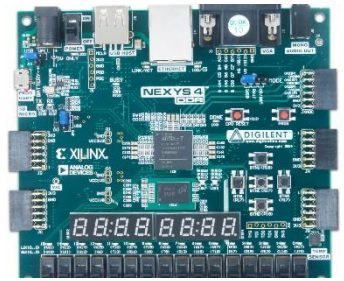
HW platform based on standard FPGA dev.kits

- Multiple boards supported (Altera, Xilinx)
- Low-cost 3rd party JTAG tools
- Open design for easy start

Software:

- Bootloader
- OS: Zephyr/FreeRTOS/Linux
- Application samples, tests, benchmarks





https://www.xilinx.com/products/boards-and-kits/1-6olhwl.html

https://www.altera.com/products/boards_and_kits/dev-kits/altera/kit-arria-v-starter.html

Open SCR1 SDKs

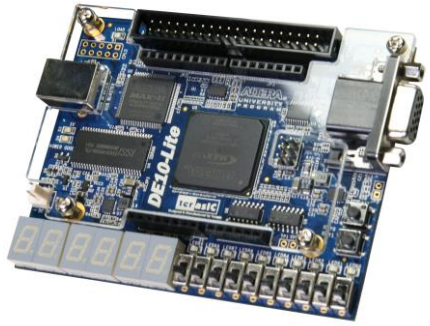
SDK platforms:

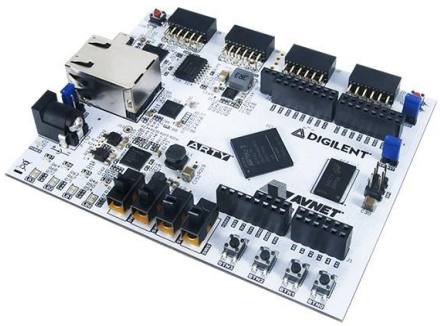
- Digilent Arty (Xilinx) @25MHz
- Terasic DE10-Lite (Intel) @20MHz
- Arria V GX Starter (Intel) @30MHz
- Digilent Nexys 4 DDR (Xilinx) @30MHz NEW
- Lattice iCE40 SOON

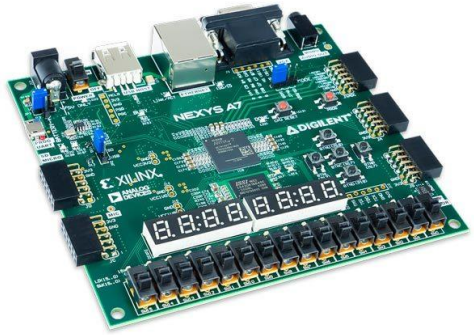
Software:

- Bootloader
- Zephyr RTOS
- Tests/SW samples

https://github.com/syntacore/scr1-sdk

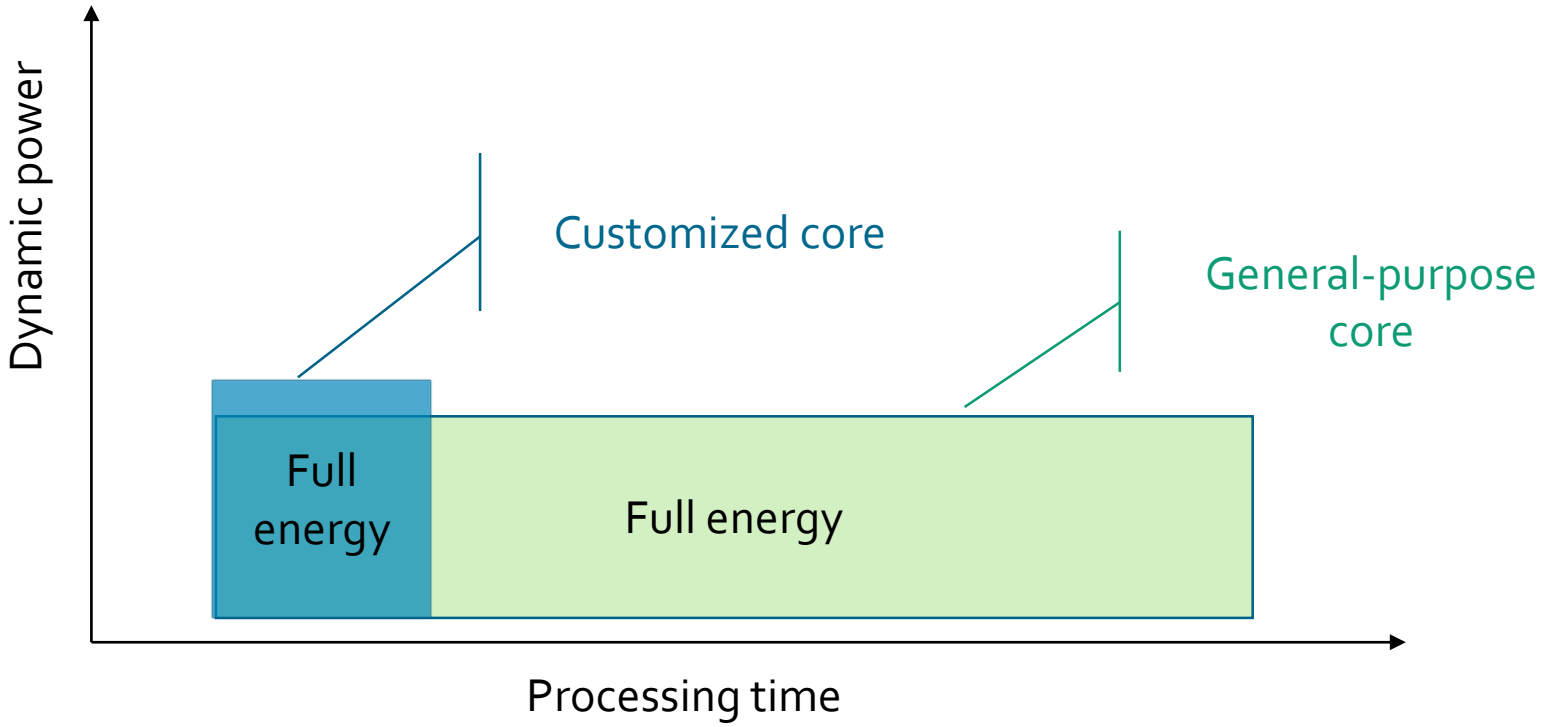






Open designs and pre-build images for a quick start, extensive guides

Extensibility/customization



Workload-specific customization

Extensibility features:

- Computational capabilities
  - New functions using existing HW
  - New Functional Units
- Extended storage
  - Mems/RF, addressable or state
  - Custom AGU
- I/O ports
- Specialized system behavior
  - Standard events processing
  - Custom events

Domain examples:

- Computationally intensive algorithms acceleration
- Specialized processors (including DSP)
- High-throughput applications
  - Wire Speed Processing/DPI/Real-time/Comms

SCRx extensibility example

Custom ISA extension for AES & other crypto kernels acceleration for SCR5

- Data
  - RV32G – FPGA-based devkit, g++ 5.2.0, Linux 4.6, optimized C++ implementation
  - Rv32G + custom – same + intrinsics
  - Core i7 6800K @ 3.4GHz, g++ 5.4.0, Linux 64, optimized C++ implementation
- 60..575x speedup @ modest area increase: 11.7% core, 3.7% at the CPU cluster level

Details in paper @EW2018 conference

Platform	Fmax, MHz	Encoding throughput, MB/s			Normalized per MHz, MB/s			RV32G + custom speed-up		
		Crypto-1	Crypto-2	AES-128	Crypto-1	Crypto-2	AES-128			
RV32G	20	0.025	0.129	0.238	0.00125	0.00645	0.0119	575.00	117.74	60.93
RV32G + custom	20	14.375	15.188	14.502	0.71875	0.7594	0.7251			
Core i7	3400	79.115	235.343	335.212	0.02327	0.06922	0.09859	30.89	10.97	7.35
Core i7 + NI	3400			3874.552			1.13957			0.64

Disclaimer: Authors are aware AES allows for more efficient dedicated accelerators designs, used as example algorithm

Getting access/evaluation

SCR1

- Is fully open: https://github.com/syntacore/scr1 and https://github.com/syntacore/scr1-sdk
- SHL-licensed with unrestricted commercial use allowed
  - Commercial SLA-based support is available

SCR 3|4|5|7

- Full package* access is available after simple evaluation agreement

For more info: evaluation@syntacore.com

(*) sufficient for evaluation and tapeout

Summary

- Syntacore offers high-quality RISC-V compatible CPU IP
  - Founding member, fully focused on RISC-V since 2015
  - Silicon-proven and shipping in volume
  - Open-source SCR1 core
    - Unrestricted commercial use allowed
    - In full wafer production
  - Turnkey IP customization services
    - with full tools/compiler support

Thank you!

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