



SiFive Overview

October 2019

FOR RISC-V 2nd week in Paris only



Silicon At The Speed Of Software



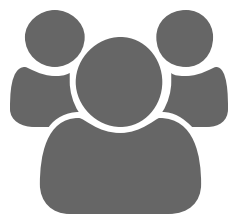
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Founded By The Inventors of **RISC-V**

SiFive's founders are the same UC Berkeley professor and PhDs who invented and have been leading the commercial implementation of the RISC-V Instruction Set Architecture (ISA) since 2010



SiFive in a nutshell



450
employees
(and hiring)



15
offices



16+
SiFive CoreIPs

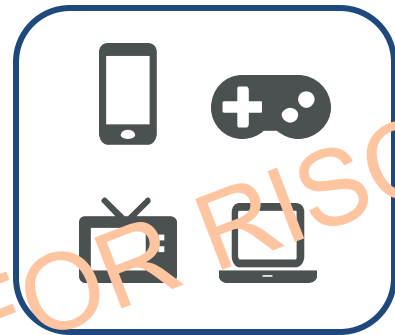
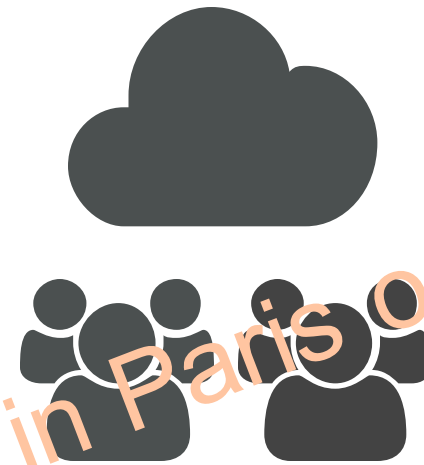


120+
design wins

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Massive Growth in Devices & Data



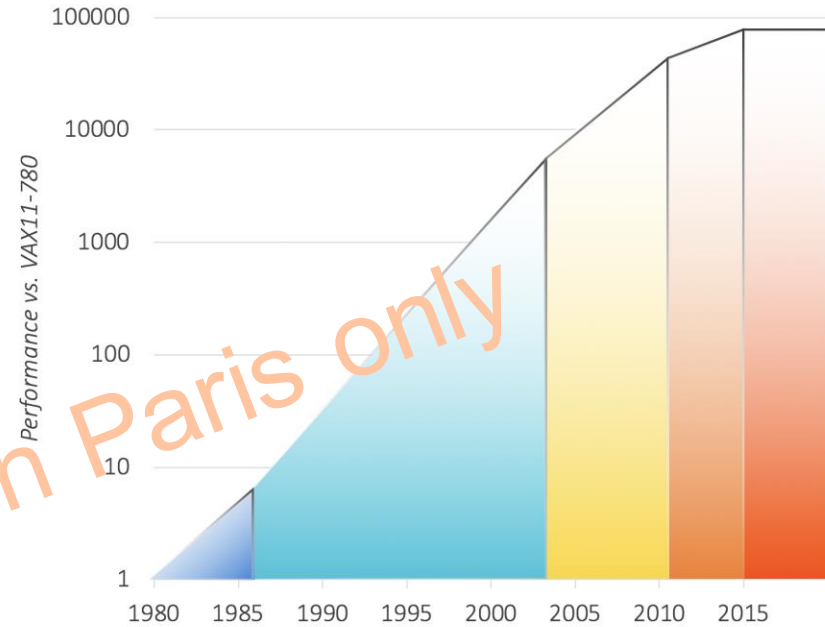
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Compute Needs Are Changing



e.g., machine learning



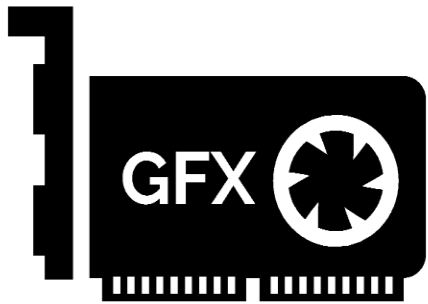
Based on [SPECintCPU](#). Source: John Hennessy and David Patterson, *Computer Architecture: A Quantitative Approach*, 6/e. 2018

But, CPUs are not getting faster!

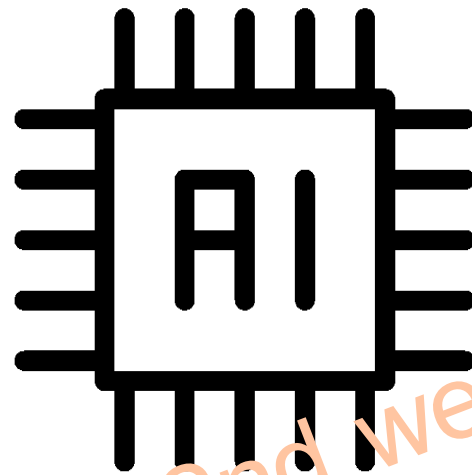
Source: Medium, *Entering the world of Machine Learning*



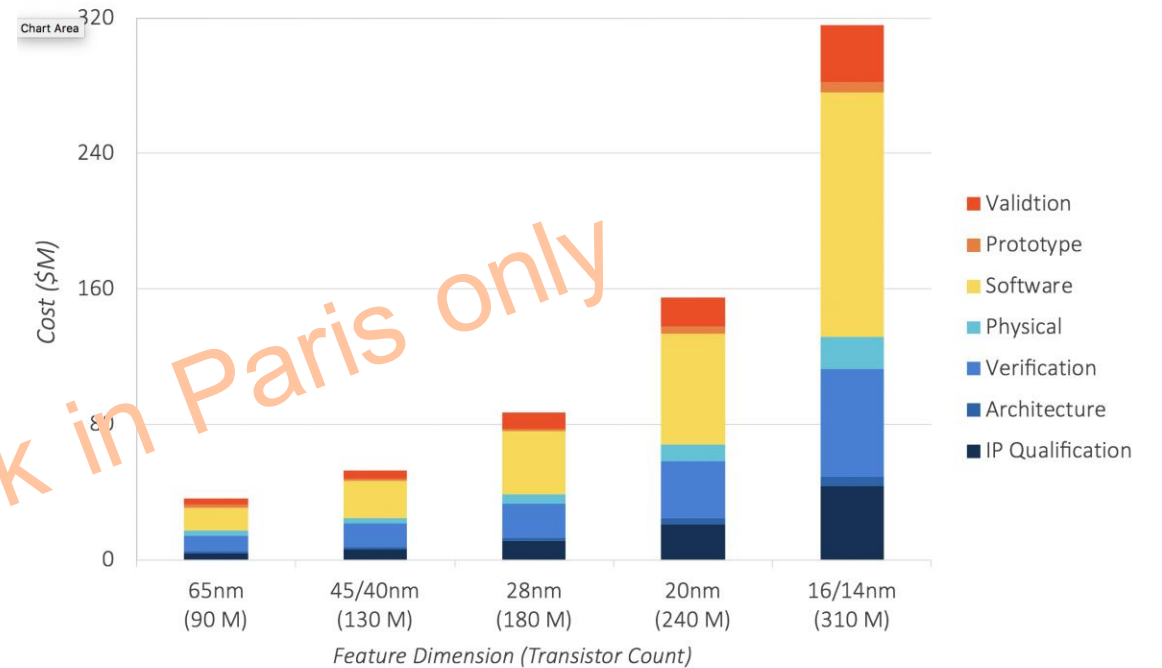
Hardware Trends: Custom Hardware To The Rescue!



GPUs



Custom Chips
(e.g., Google TPU)



But, custom chip development costs are too high!

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SiFive Core IP RISC-V Configurable Cores

	E Cores 32-bit embedded cores MCU, edge computing, AI, IoT	S Cores 64-bit embedded cores Storage, AR/VR, machine learning	U Cores 64-bit application cores Linux, datacenter, network baseband
7 Series	E7 Series	S7 Series	U7 Series
Highest performance: 8-stage, dual-issue superscalar pipeline	<ul style="list-style-type: none"> > E76-MC Compare to Cortex-M7 Quad-core 32-bit embedded processor > E76 Compare to Cortex-M7 High performance 32-bit embedded core 	<ul style="list-style-type: none"> > S76-MC No 64-bit Cortex equivalent Quad-core 64-bit embedded processor > S76 No 64-bit Cortex equivalent High-performance 64-bit embedded core 	<ul style="list-style-type: none"> > U74-MC Compare to Cortex-A55 MP4 Multicore for U74 cores and one S76 core > U74 Compare to Cortex-A55 High performance Linux-capable processor
3/5 Series	E3 Series	S5 Series	U5 Series
Efficient performance: 5-6-stage, single- issue pipeline	<ul style="list-style-type: none"> > E34 Compare to Cortex-R5F E31 features + single-precision floating point > E31 Compare to Cortex-R5 Balanced performance and efficiency 	<ul style="list-style-type: none"> > S54 No 64-bit Cortex equivalent S51 features + single-precision floating point > S51 No 64-bit Cortex equivalent Low-power 64-bit MCU core 	<ul style="list-style-type: none"> > U54-MC Compare to Cortex-A53 Multicore application processor with four U54 cores and one S76 core > U54 Compare to Cortex-A53 Linux-capable application processor
2 Series	E2 Series	S2 Series	
Power & area optimized: 2-3-stage, single- issue pipeline	<ul style="list-style-type: none"> > E24 Compare to Cortex-M4F E21 + single-precision floating point > E21 Compare to Cortex-M4 E20 + User Mode, Atomics, Multiply, TIM > E20 Compare to Cortex-M0+ Our smallest, most efficient core 	<ul style="list-style-type: none"> > S21 No 64-bit Cortex equivalent Area-efficient 64-bit MCU core 	



SiFive Cloud Services

- SiFive Core Designer
- Click to configure a RISC-V Core!
- RTL download in 24hrs!
- Core IP configured to your needs!

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The screenshot shows the configuration interface for a U7 Series core. The main configuration area is titled "Modes & ISA" and includes the following settings:

- Modes & ISA:** Number of Cores is set to 1.
- Privilege Modes:** Machine Mode and User Mode are both checked.
- ISA Extensions:** Multiply (M Extension) and Atomics (A Extension) are checked. Floating Point is set to "Double FP (F & D)".
- Extensions:** SiFive Custom Instruction Extension (SCIE) is unchecked.

The right-hand side of the interface displays the "U7 Series Core Complex" configuration, which includes:

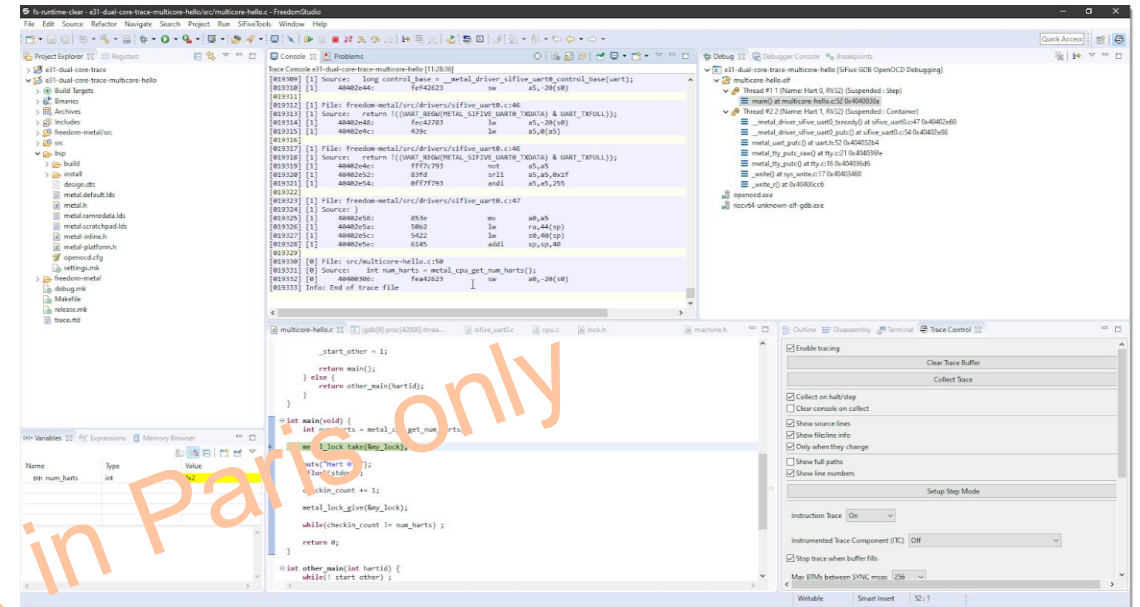
- U7 SERIES CORE:** 1 Core, RV64IMAFDC. Machine Mode, User Mode, Multiply, Atomics, FP (F & D), No SCIE, 0 Local Interrupts.
- Perf. Optimized Branch Prediction**
- Clock Gating:** PMP 8 Regions.
- Instruc. Cache:** 32 KiB - 8-way.
- Data Cache:** 32 KiB - 8-way.
- Instruc. TIM:** None.
- Data Loc. Store:** None.
- No Instruction Trace - 2 Perf Counters**
- Front Port:** 64-bit AXI4.
- System Port:** 64-bit AXI4.
- Peripheral Port:** 64-bit AXI4.
- Memory Port:** 128-bit AXI4.
- L2 Cache:** 128 KiB, 8-way, 1 Bank.
- Debug Module:** JTAG - SBA, 2 HW Breakpoints, 0 Ext Triggers.
- PLIC:** 7 Priority Levels, 127 Global Int.
- CLINT:**

At the bottom right, there is a "Review" button and a "Base: U74 Standard Core" link. An "On-Chip Memory" button is also visible at the bottom of the configuration area.



Quarterly updates

- SiFive delivers IP and product updates on a quarterly basis
- Q3 Update includes Nexus 5001 trace encoders
- SiFive Freedom Studio support
- Open Source RISC-V Trace Decoder now on github

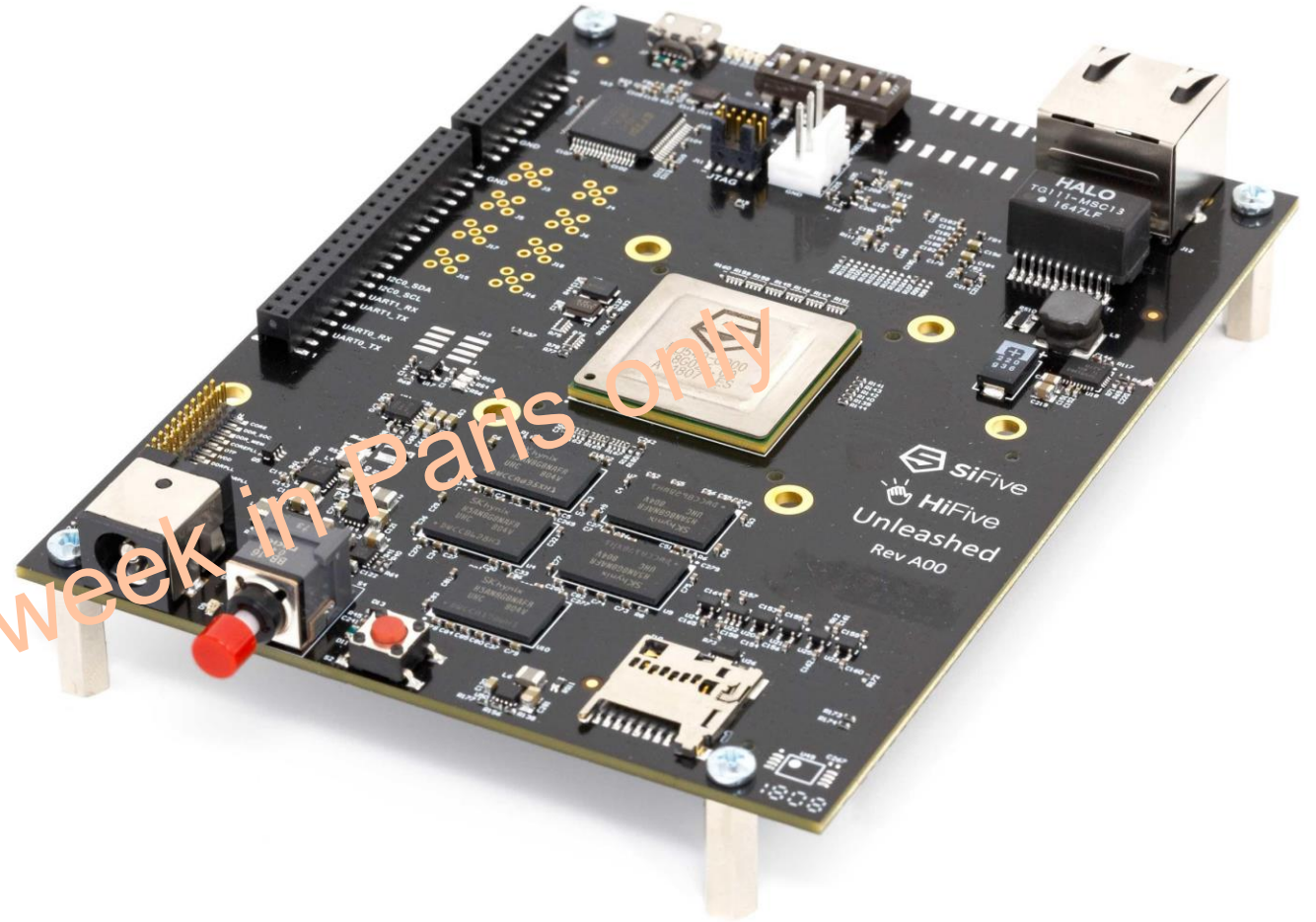


SiFive Freedom Studio

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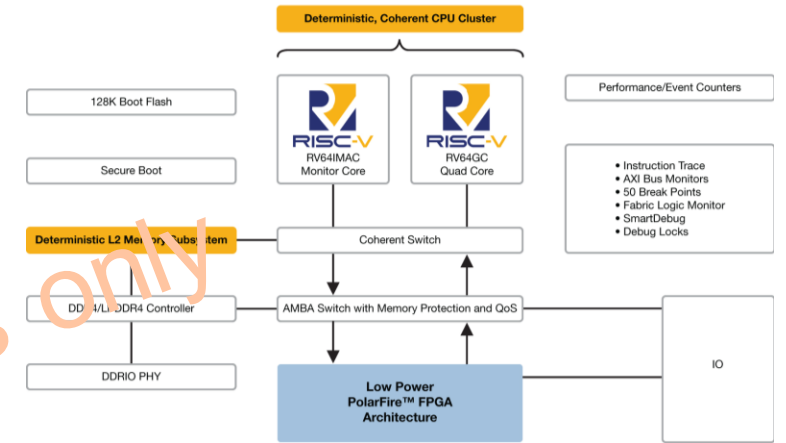


- HiFive Unleashed
 - Quad Core Linux Capable CPU
 - Available via CrowdSupply
- SiFive World Tour
 - 50-City Tour
 - SiFiveTechSymposium.com





SiFive Commercial Success



huami

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FADU





SoC security best practices



Avoid fragmented security solutions



Get rid of legacy security



Get a Root-of-Trust

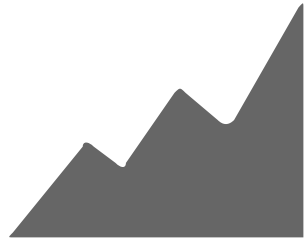


Improve auditability

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RISC-V SoC needs more security



**Scalable
architecture**



**Enhanced
isolation**



**Finer grained
controls**



**System level
security**

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**Linley Fall
Processor
Conference 2019**

Santa Clara, CA., USA

October 23rd & 24th

Join SiFive CTO, Yunsup Lee, and Security Director, Dany Nativel, for the latest innovations and updates on SiFive architectures!