Scientific Day :
RISC-V for critical embedded systems

IRT Saint-Exupery & GDR SOC2

- **IRT Saint-Exupéry**
  - Public/Private technological research center in Aeronautics, Space, and Safety-Critical Systems
- **GDR SOC2**
  - National academic network on *System-On-Chip, Embedded Systems, and Connected Objects*
  - 1,400+ members from 64 french research units
- **IRT SE + GDR SOC2**
  - We join forces each year to organize a scientific day gathering academia and industry in the field of critical embedded systems
  - 2017 : AADL for the co-design of hardware-software embedded systems
  - 2018: Hardware interference and timing determinism for modern SoCs
  - **2019 : RISC-V for critical embedded systems**

RISC-V for critical embedded systems

- In a context of economical war, industrial development of RISC-V could be an important step toward technological sovereignty in Europe.
- What does the industry of critical embedded system expect from the RISC-V ecosystem?
  - How to reach RISC-V industrialization in safety critical systems with conformance to safety standard?
  - How RISC-V ecosystem can contribute to the embeded AI challenge for safety critical mission ?
- During the day, among other points, we will try to discuss:
  - Does an open achitecture ease architecture evaluation and safety demonstration (virtual platform, formal verification, failure analysis, …)?
  - Does an open architecture make it easier to develop and integrate application specific extensions (radiation protection, hardware acceleration, …)?

Program overview

Michael Chapman (CORTUS)	*RISC-V in embedded applications*
Antoine Certain (Airbus Defence & Space)	*What does the space industry expect from RISC-V?*
Johan Klockars (Cobham Gaisler)	*Development of a RV64GC IP core for the GRLIB IP Library*
Denis Dutoit (CEA Leti & EPI)	*European Processor Initiative: First steps towards a made-in-Europe high-performance microprocessor*
Eric Jenn (IRT Saint-Exupéry)	*Achieving determinism and performance on the RISC-V FlexPRET Processor*
Daniel Große (University of Bremen & DFKI GmbH)	*RISC-V based Virtual Prototype: An Open Source Platform for Modeling and Verification*
Romain Soulat (Thalès Research & Technology)	*Formal Verification of RISC-V Implementation Designs*

Practical informations : location

- Location : Jussieu Campus
- Metro line 7 or 10, station Jussieu
- 15 minutes walk from here, crossing the *Seine* and then through the *Jardin des plantes*
- Once on the campus :
  - Follow the arrows
  - Room 105, corridor between tower 25 and 26, 2nd floor
  - Stairs or Elevator (push button 1 because 2nd floor is 1st *étage* in french*)*
  - If you are registered, you must have received an email with a map of the campus

Practical informations : schedule

- Welcome coffee from 9am
- Lunch break from midday to 2pm
  - No onsite accomodation was possible but there are many restaurants and foodtrucks around the campus, especially rue Linné
- Closure at 5:15pm