

**S**ystem **O**n **C**hip  
embedded **S**ystems  
and **cOnneCted** things

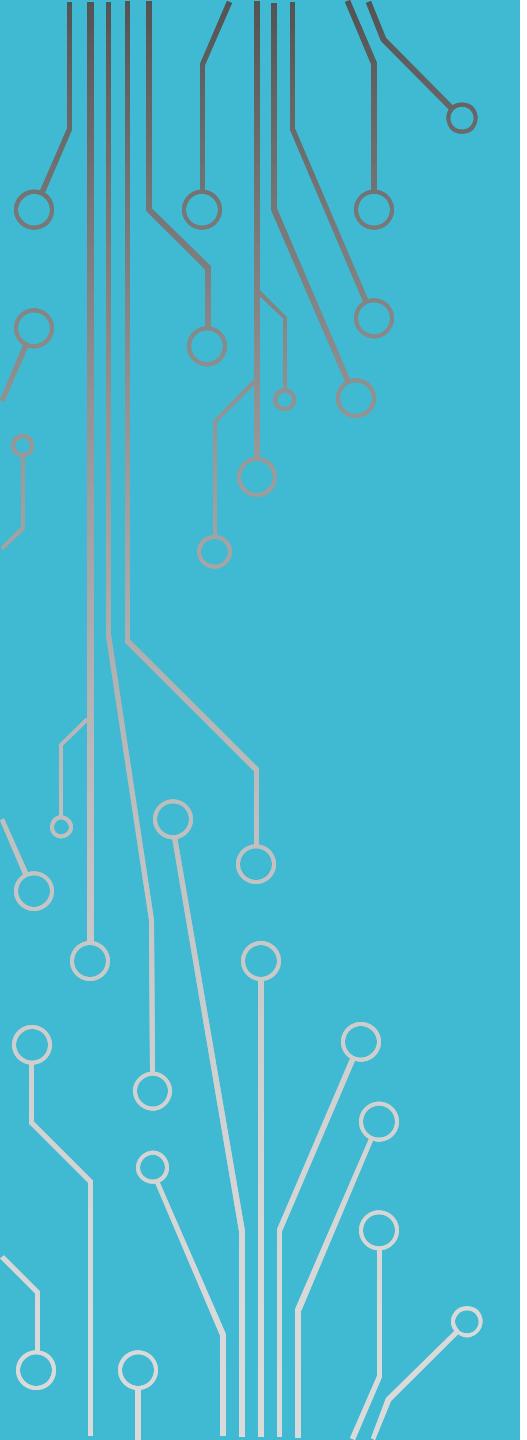
## GdR SOC<sup>2</sup>

<http://www.gdr-soc.cnrs.fr/>



Director: Ian O'Connor

Vice-Directors: Cristell Maneux, Sébastien Pillement, Patrick Girard



# The GdR in action

- A CNRS GdR<sup>\*</sup>'s missions
  - bring a research community together
  - act as CNRS contact point for a **field of research**
- GdR SOC<sup>2</sup>'s specificities
  - high percentage of academic staff, several small teams
  - strong interaction with industry
  - at the intersection of 3 National University Council sections and two CNRS institutes

\* GdR = research network

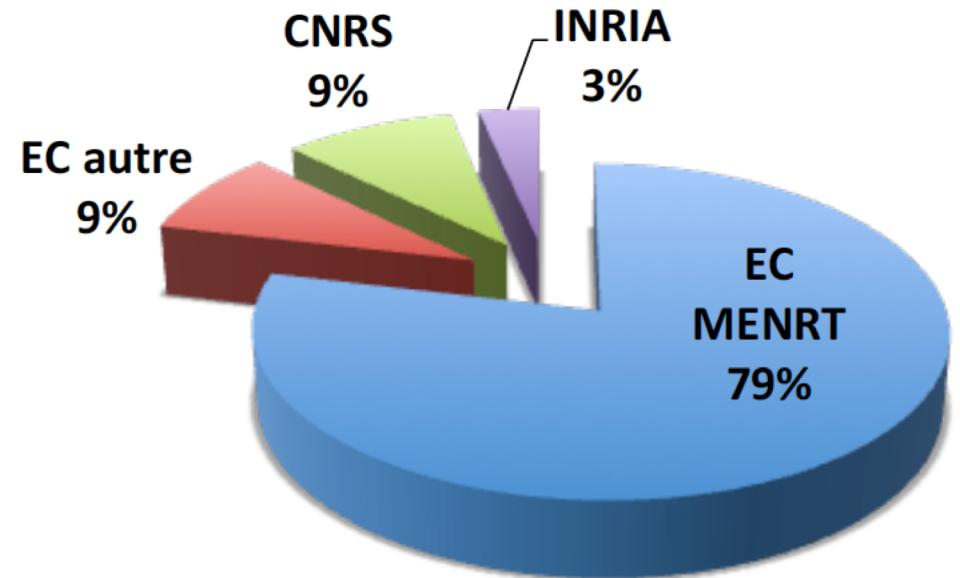


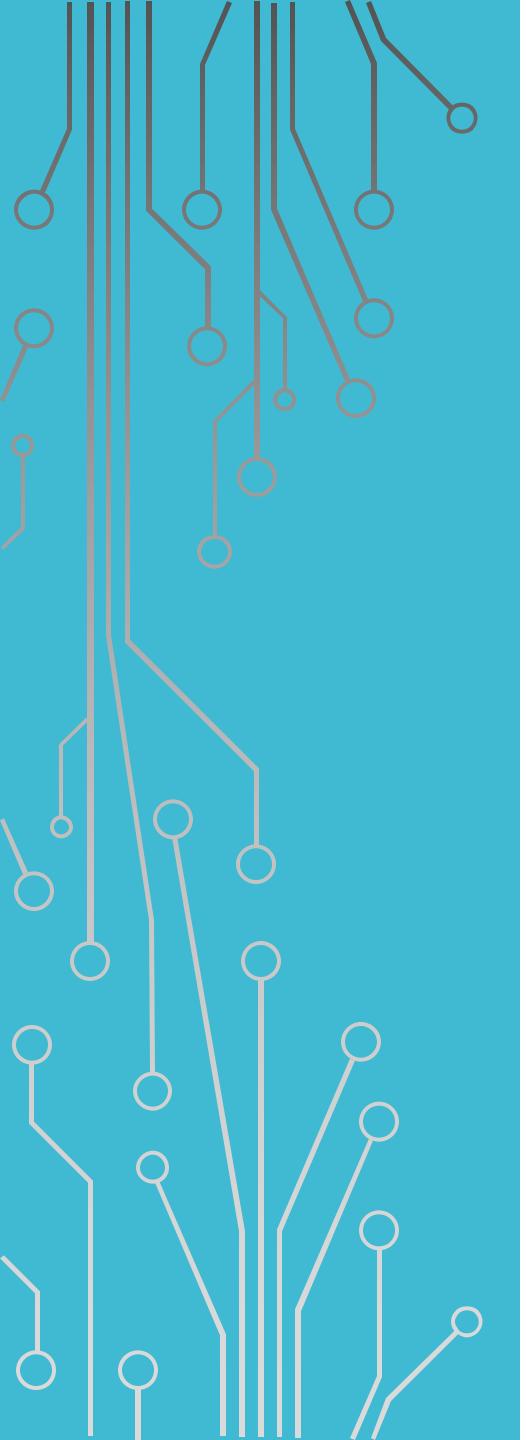
GdR SOC<sup>2</sup> – System On Chip, Systèmes embarqués et Objets Connectés<sup>2</sup>

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# The GdR in action

- Unite
  - 56 research labs
  - >600 permanent staff





# The GdR in action

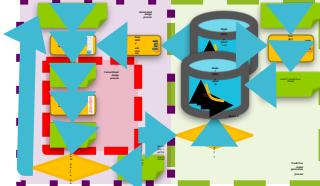
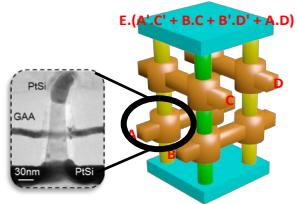
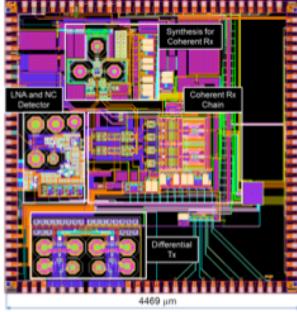
- **Drive**

- 15 research theme days per year,
- barcamps,
- Co-organized research seminars (with IEEE-CAS, IRT Saint-Exupéry, Pole AerospaceValley)
- Support 2 short-term research schools
- National Research Days Montpellier, 19-21 June 2019 (**next one 23-25 June 2020 in Rennes**)
- Research theme of the year

# The GdR in action

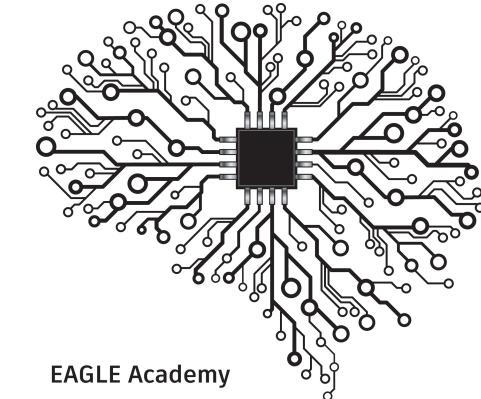
- Organize

- 3 thematic topics
  - Embedded high-performance computing
  - Cyberphysical frontiers and interfaces
  - System security and integrity
- 3 cross-thematic topics
  - Smart devices
  - Future technologies
  - Methods and tools
- To be announced : AI



# SOC<sup>2</sup> and AI

- Foundations and technologies
  - neuroinspired (spiking, STDP)
  - non-volatile memories
  - analog implementation etc.
- Applications and architectures:
  - hardware accelerators for inference
    - IoT / CPS, vision, wearables, edge computing
  - software techniques (compression etc.)
  - dynamic control of systems
- Methods and tools
  - CAD & AI: the tools of tomorrow
- AI and security
  - attacks, reverse engineering etc.

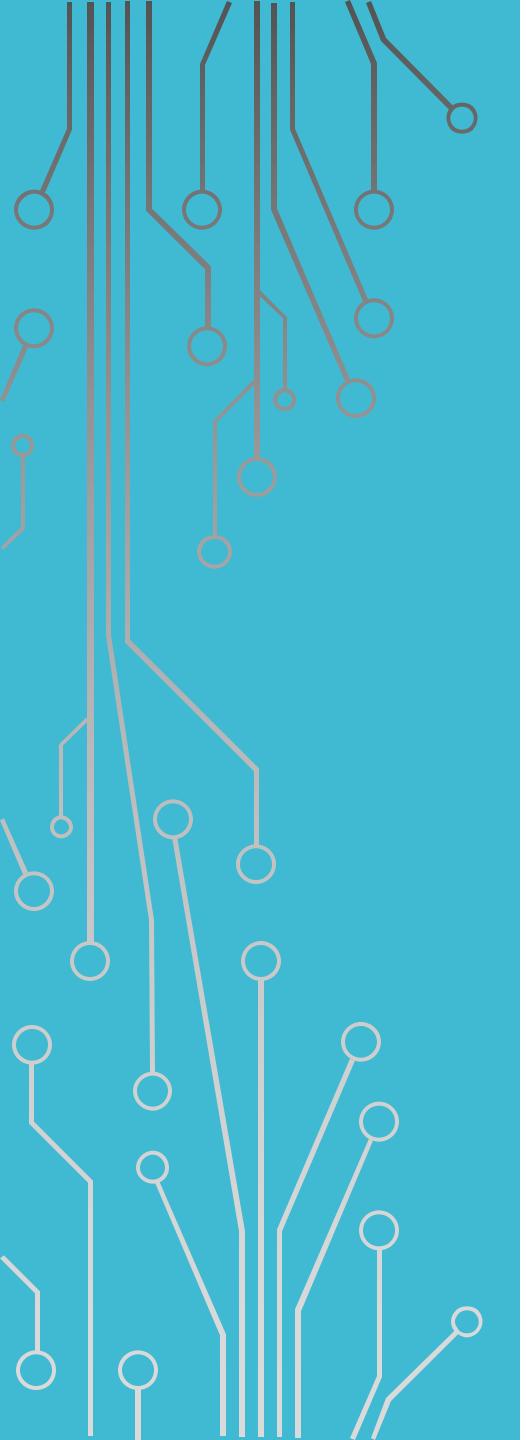




# SOC<sup>2</sup> and RISC-V

- Expectations of the industry in term of modern architecture for critical embedded systems and how could RISC-V-based systems fullfil these requirements.
- Design RISC-V-based architectures for (critical) embedded systems.
- Modeling and formal verification of RISC-V-based architectures.
- Design and tools for RISC-V

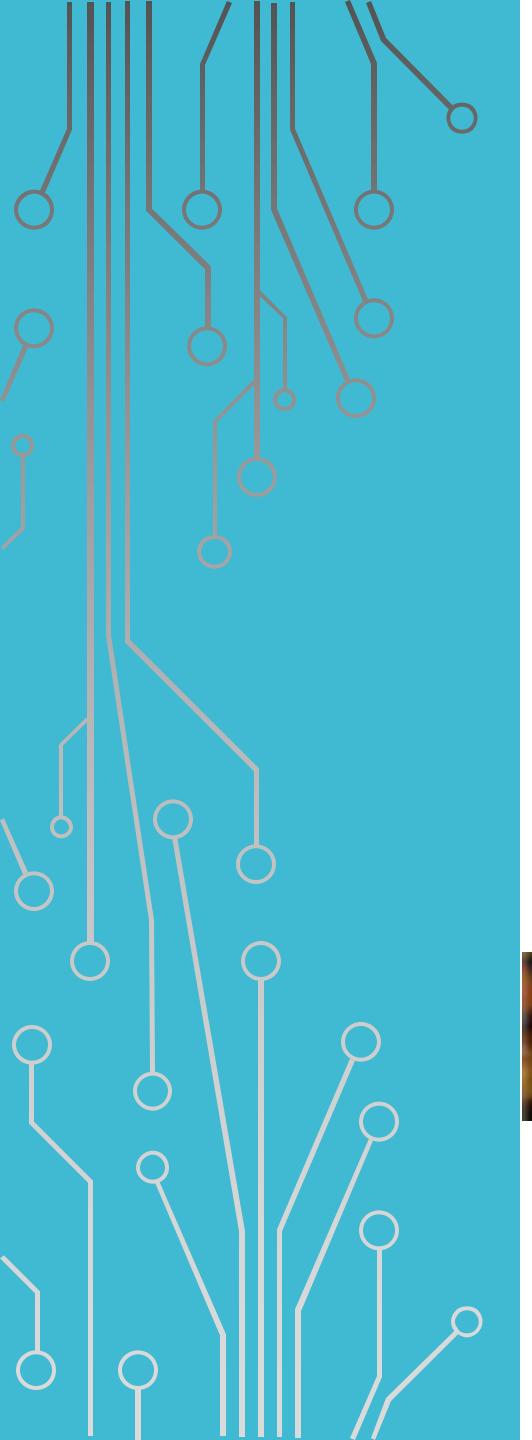




# A GdR in its ecosystem

## Partner Companies club

- Represent industrial partners
  - advice on topics, proposals for research theme days
- Services for industrial partners
  - database of contacts, research lab survey, training and course survey
  - access to research theme days
  - access to lab software tools (if IP protected)
  - dissemination of messages or offers (internship, thesis ...)
  - standard CNRS convention
- Financial aspects
  - SME contributions, large groups
  - free access for startups



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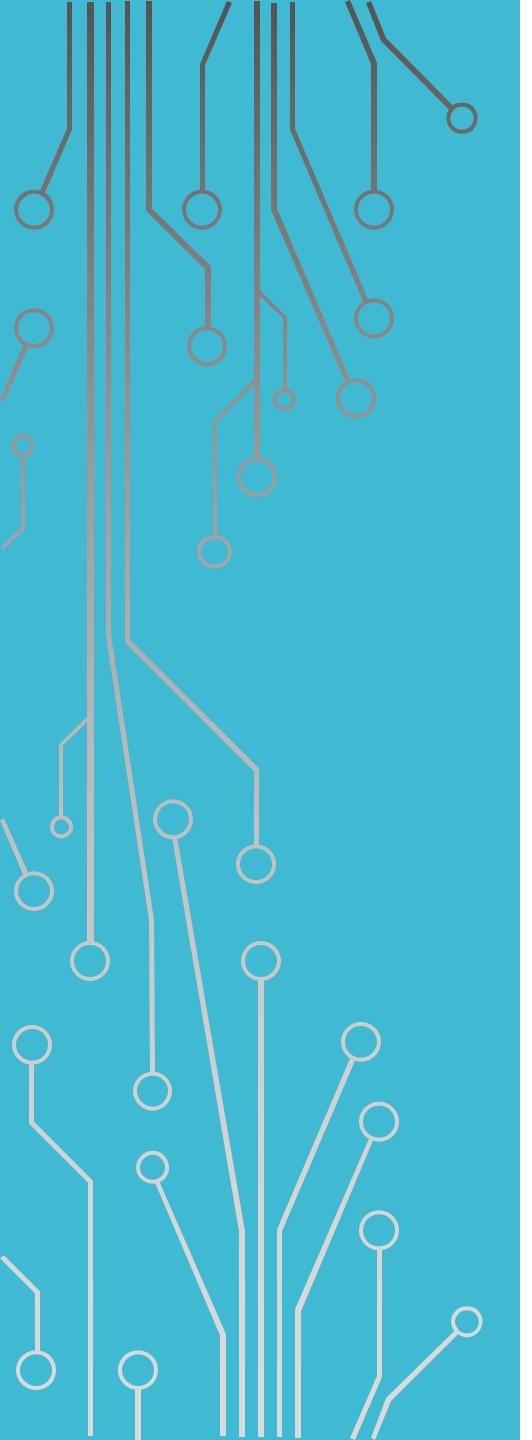
**Join us**

<http://www.gdr-soc.cnrs.fr/>



# Embedded high-performance computing

- Towards ultra-high performance and ultra-low power embedded systems
  - hardware and software optimization
  - alternative computing approaches
  - technology integration
- Safe and predictable massively parallel embedded computing
  - programming models and compilation techniques
  - allocation and scheduling
  - operating safety



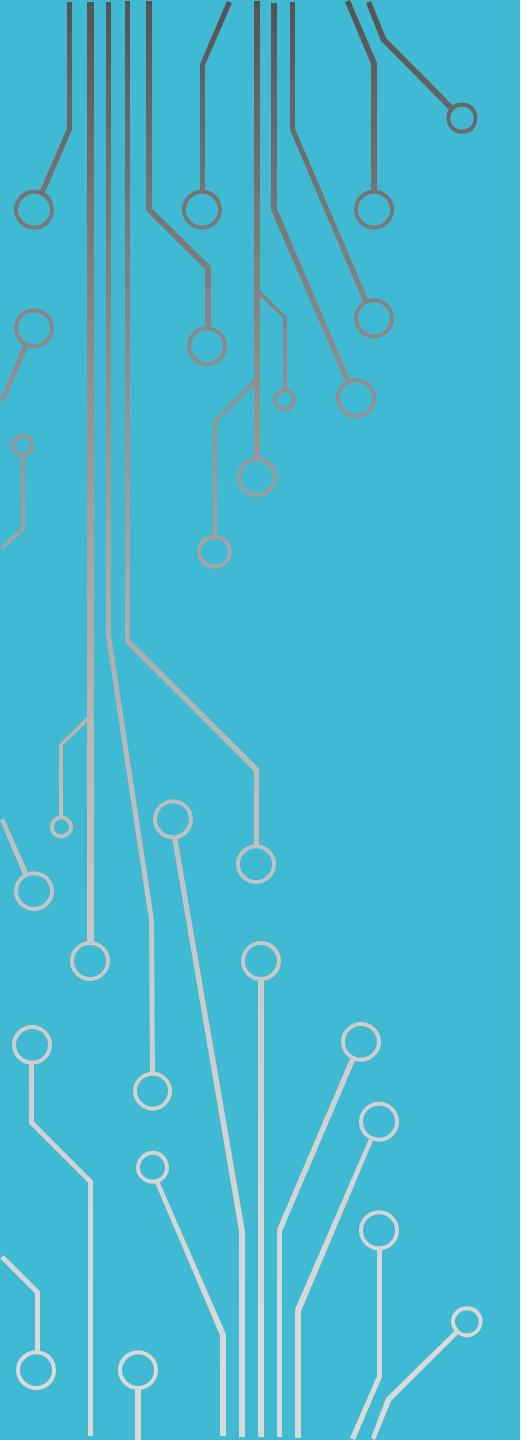
# Cyberphysical frontiers and interfaces

- Integrate energy-efficient intelligence into sensors
  - optimize the sensor and the interface
  - efficient RF transmission
  - adapt the node to the application
  - compress data locally
- Optimize communication with the heart of the system
  - interoperable RF communications
  - secure communications
- High-level multi-domain modeling



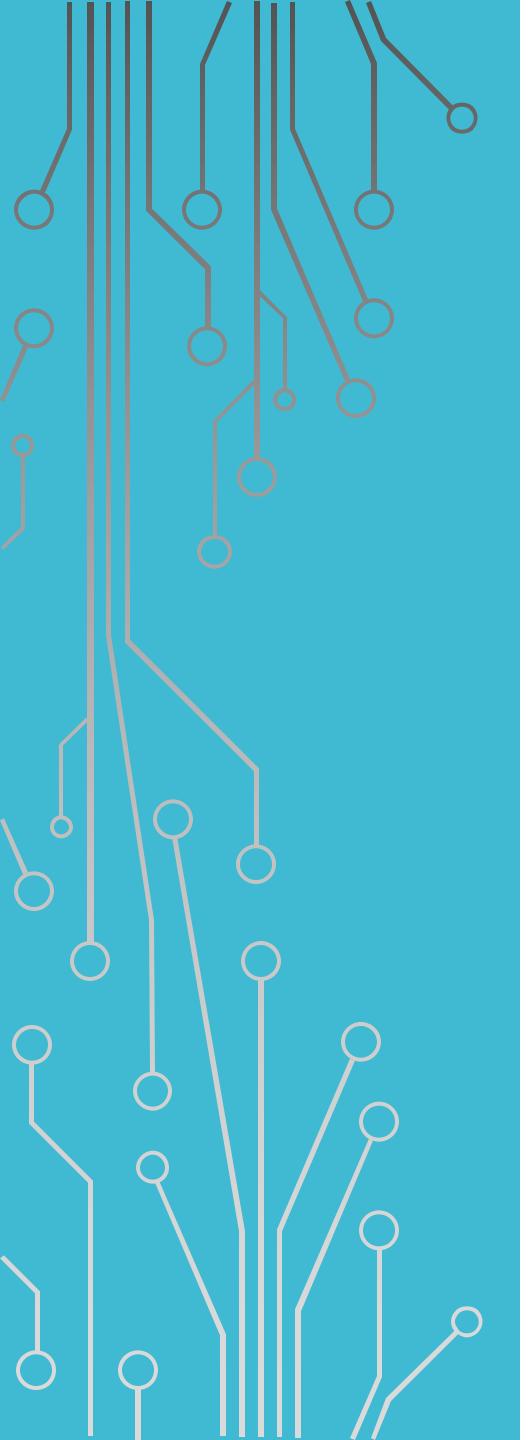
# System security and integrity

- Adapt security methodologies
  - to future technologies (3D integration, nanoelectronics, ultra low-power, mixed-signal ...)
  - to high levels of abstraction for the seamless insertion of developed methods (formal verification, security, fault tolerance, ...) into design flows
  - to scale in terms of complexity, integration density, software and hardware fusion, and system heterogeneity



# Smart devices

- Scale up networks of smart devices and dataflow
- Architectures and operating modes
- Applications:
  - traffic improvement, road safety, continuity of service
  - deploying increasing numbers of *in vivo* smart devices
  - pain reduction
  - ubiquity - smart territory, industry 4.0
  - ethical, social issues



# Future technologies

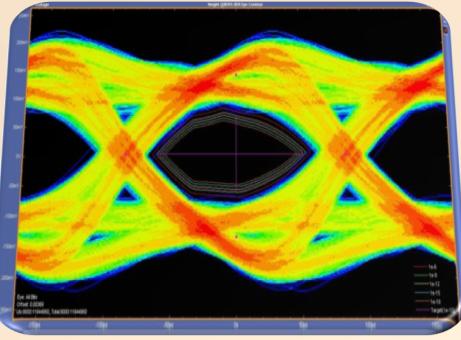
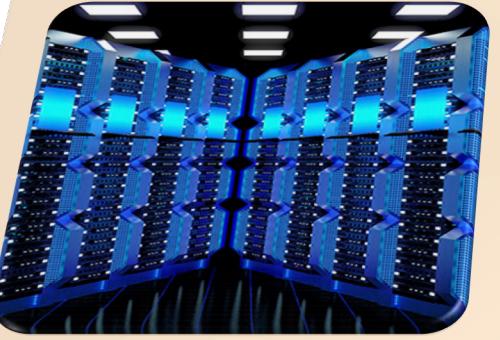
- Functions
  - computing (nanowires, nanotubes, SET ...)
  - memory (MRAM, ReRAM, FeRAM ...)
  - interconnect and communication (nanophotonics, spin, THz, visible-range optics ...)
- To improve
  - SoC energy efficiency, evolution of computing architectures
  - memory integration density
  - communication data rate
- New computing paradigms (bio-inspired, approximate, stochastic ...)



# Methods and tools

- Hardware / software co-design of parallel many-core architectures
- Holistic analog / digital-software approach, modeling and multi-physics simulation
- Modeling for fault tolerance and resilience
- Adapt methods to new technologies and new computing paradigms

# Topic structure



*Embedded high-  
performance  
computing*

**Cyberphysical  
frontiers and  
interfaces**

**System  
security and  
integrity**

**Smart devices**

**Future technologies**

**Methods and tools**

