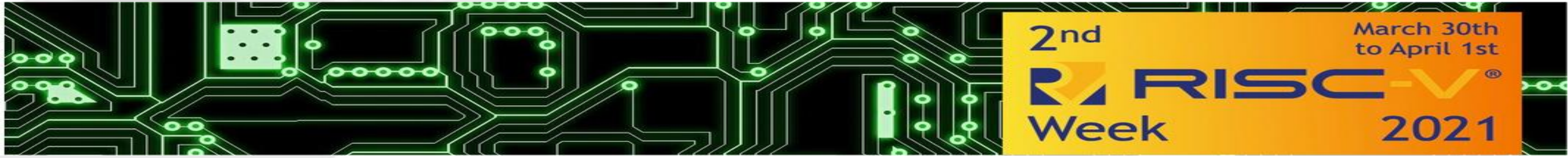

CMP Services for ASIC Prototyping, An Overview

Kholdoun TORKI

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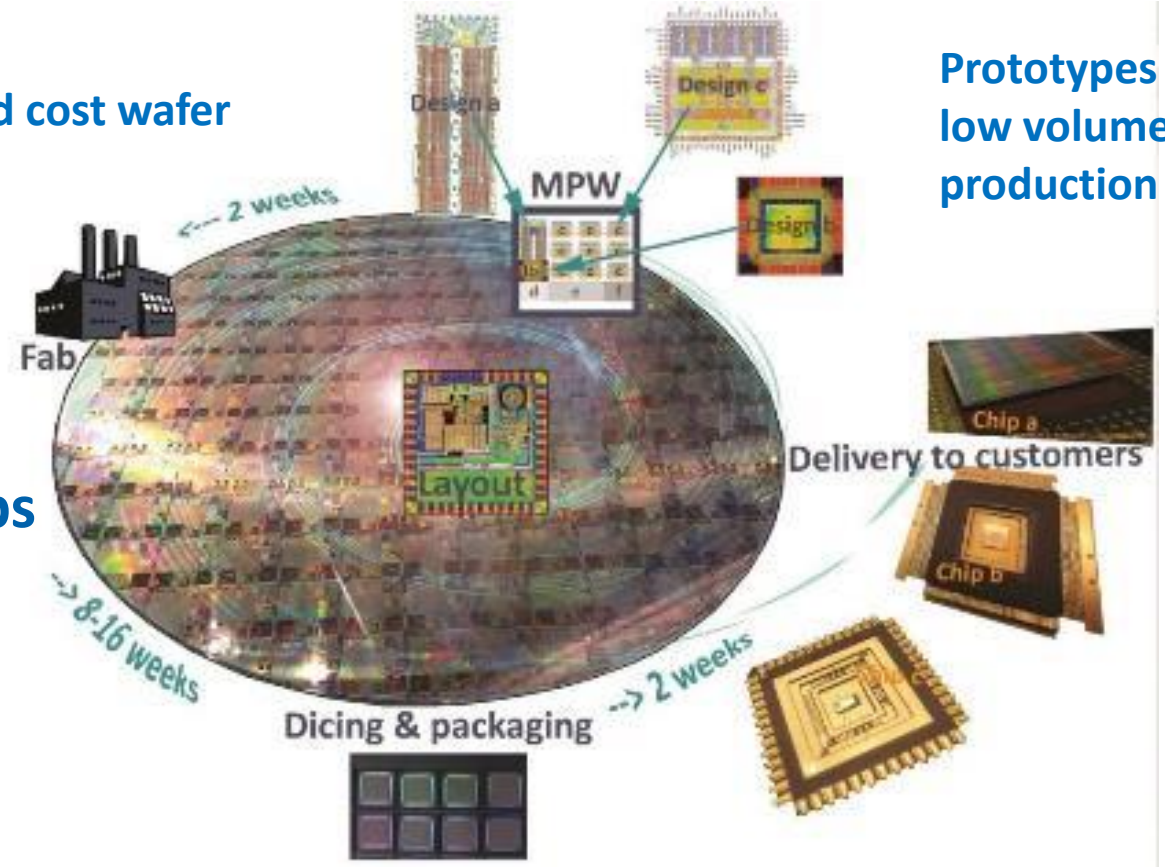
Horizon 2020
European Union funding
for Research & Innovation

MPW services for prototyping and Low Volume Production

CMP makes available and affordable **advanced CMOS, MEMS, Photonics technologies** as well as **mature and/or niche market technologies** to cover a wide range of applications.

Shared cost wafer

Prototypes or low volume production



Affordable prototyping service

CMP shares manufacturing cost of ICs prototyping and small volumes.

From layout to chips

Technical supports

CMP provides supports & training for Design Kit implementation and usage

CMP offers several companion services for packaging and test.

Technology Portfolio in 2021 (1/2)

IC

ams	0.35µ CMOS 4LM 0.35µ CMOS-Opto 4LM	0.35µ SiGe 4LM 0.35µ HV-CMOS (50V / 120V)
ST	65nm CMOS 7LM 130nm CMOS 6LM 130nm HV-CMOS 4LM	28nm FDSOI 130nm SOI - FEM 0.16µ BCD-SOI	55nm SiGe BiCMOS 130nm SiGe BiCMOS 0.16µ BCD
ON Semi	0.18µ CMOS 5LM 0.35µ CMOS 4LM	0.18µ HV-CMOS (45/70V) 0.35µ HV-CMOS (25/50V)
EM Microelectronic	0.18µ CMOS 5LM (ULP / ULV)	

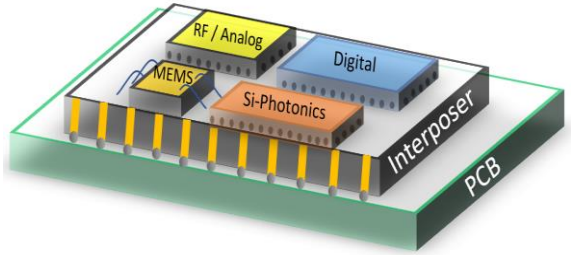
MEMS

CMP / ams	0.35 µ CMOS front-side bulk micromachining		
MEMSCAP	PolyMUMPS	SOIMUMPS	PiezoMUMPS

Technology Portfolio in 2021 (2/2)

Photonics	CEA-LETI	Silicon Photonics / Si310-PHMP2M
	AMF / CMC	Silicon Photonics
	TEEM Photonics	Photonics on Glass

3D-IC	CEA-LETI	UBM, micro-bumps, RDL, TSV / 3D assembly / Open3D
	ams	0.35um 4 LM Active or Passive Interposer + UBM
	ams	UBM + Bumps at Wafer Level on 0.35µ
	ST	UBM + Copper pillar at Wafer Level (processes on 300mm wafers)
	ON Semi	Passive Interposer + UBM



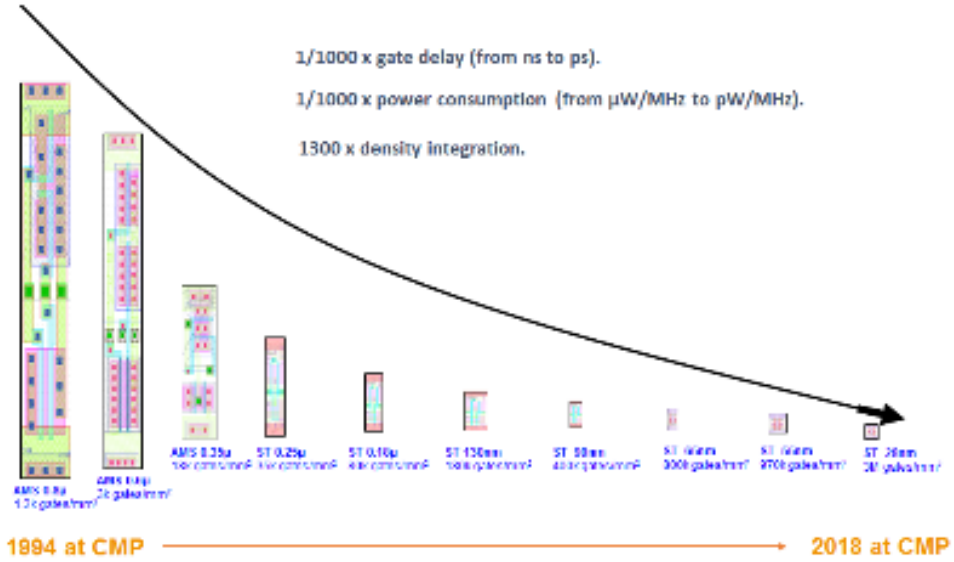
History of CMP technology portfolio

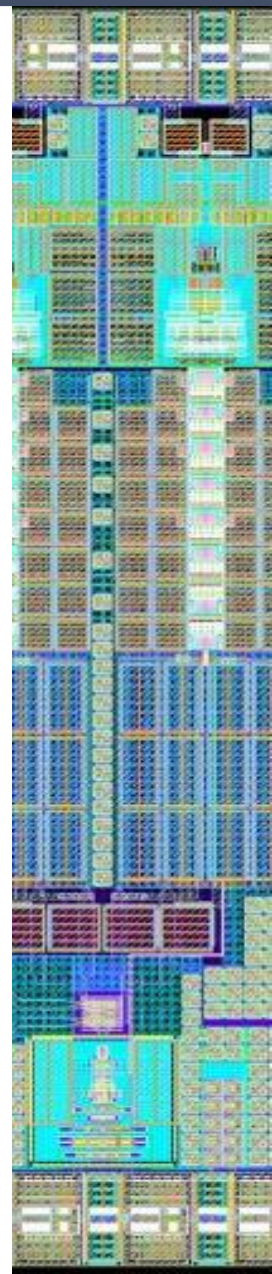
1981 : launching CMP with NMOS
1983 : development of NMOS / launching CMOS
1984 : development of CMOS
1987 : abandon NMOS / increase the frequency of CMOS runs
1990 : launching Bipolar / BiCMOS / MESFET GaAs / HEMT GaAs / advanced CMOS (0.5µm TLM)

1995 : launching CMOS / BiCMOS and GaAs compatible MEMS / DOEs / deep-submicron CMOS (0.25µm 6LM)
1998 : launching surface micromachined MEMS / abandon MESFET GaAs
1999 : launching SiGe / 0.18µm CMOS
2001 : 0.35µm HBT SiGe BiCMOS
2003 : 130nm CMOS
2003 : PolyMUMPS / MetalMUMPS / SOIMUMPS
2004 : 90nm CMOS
2005 : ASIMPS / SUMMIT / SANDIA

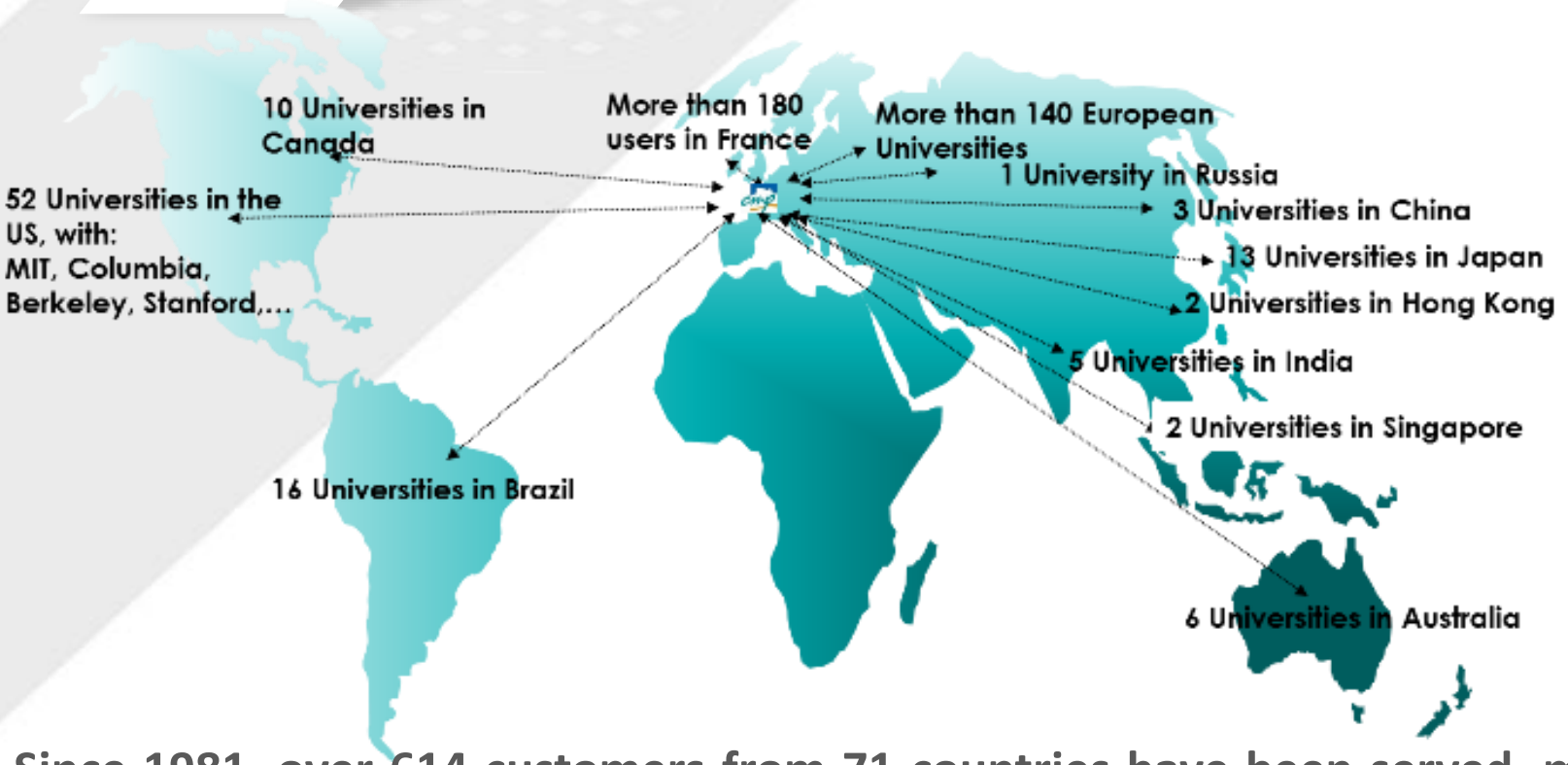
2006 : 65nm CMOS GP
2008 : 45nm CMOS / 65nm SOI
2009 : 40nm CMOS
2010 : 130nm 3D-IC / 20nm FDSOI
2011 : 28nm CMOS / 150nm GaAs pHEMT / 180nm CMOS CIS

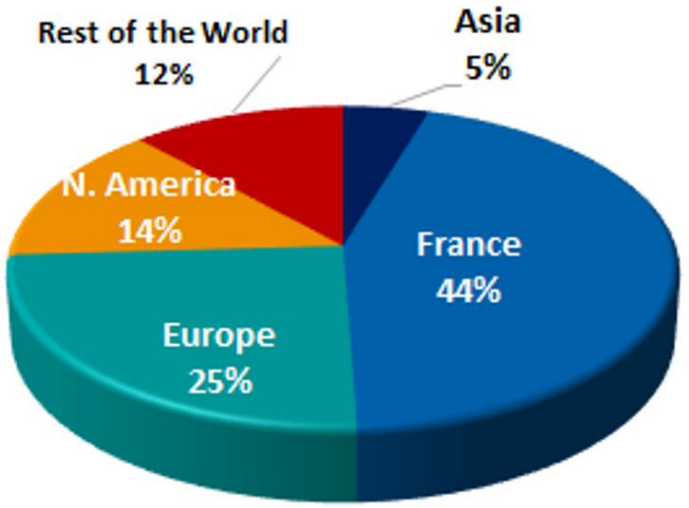
2012 : 28nm FD-SOI / 0.18µm CMOS/HV-CMOS
2013 : Analog 130nm H9A CMOS / THELMA MEMS
2014 : 30nm SOI FEM / Bulk micromachining / DALSA MEMS / PiezoMUMPS
2015 : 160nm BCD8sP / Micralyne MEMS / Open 3D CEA / 55nmBiCMOS
2016 : CEA Si-Photonics / active and passive interposers
2017 : 160nm BCD8s-SOI
2018 : EU Mirphab Pilotline / CEA MAD200 OxRAM NVM
2019 : ON Semi / AMF / EM
2020 : SMIC / TEEM Photonics





Worldwide service & partnership





Distribution of circuits per geographical area in 2020

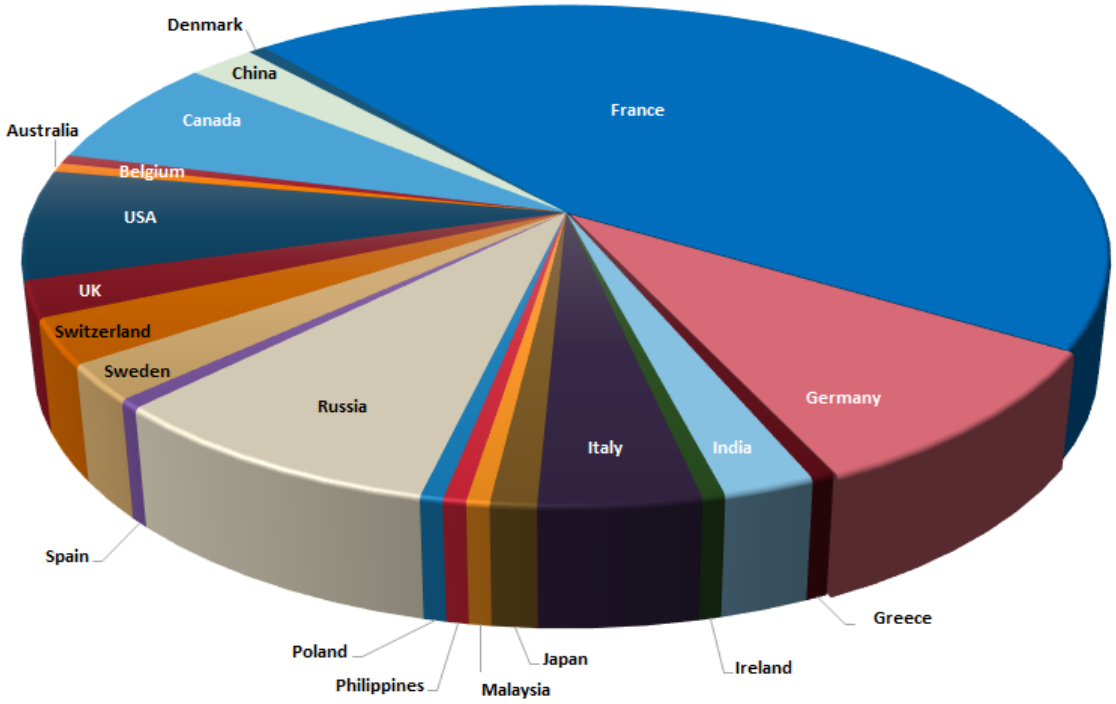
Since 1981, over 614 customers from 71 countries have been served, more than 8100 projects have been prototyped through 1043 MPW runs and 74 different technologies have been interfaced.

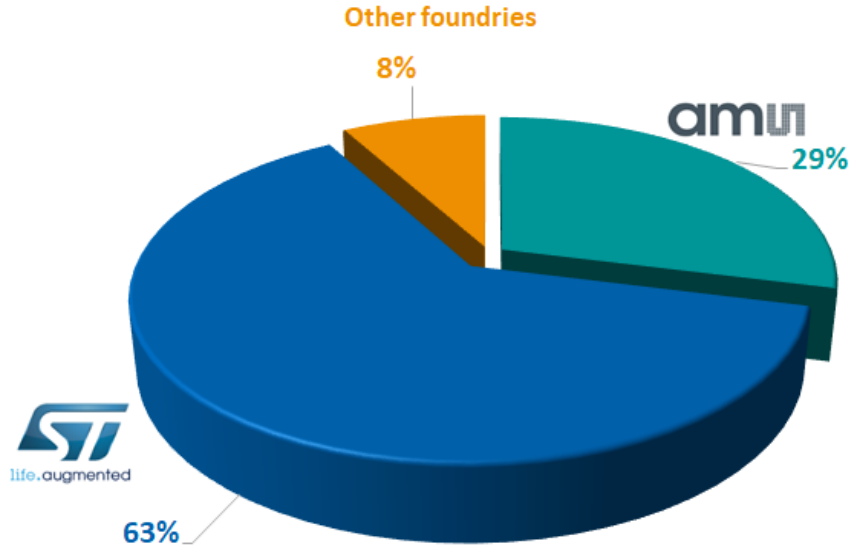
Since 2019, CMP is partner in EUROPRACTICE

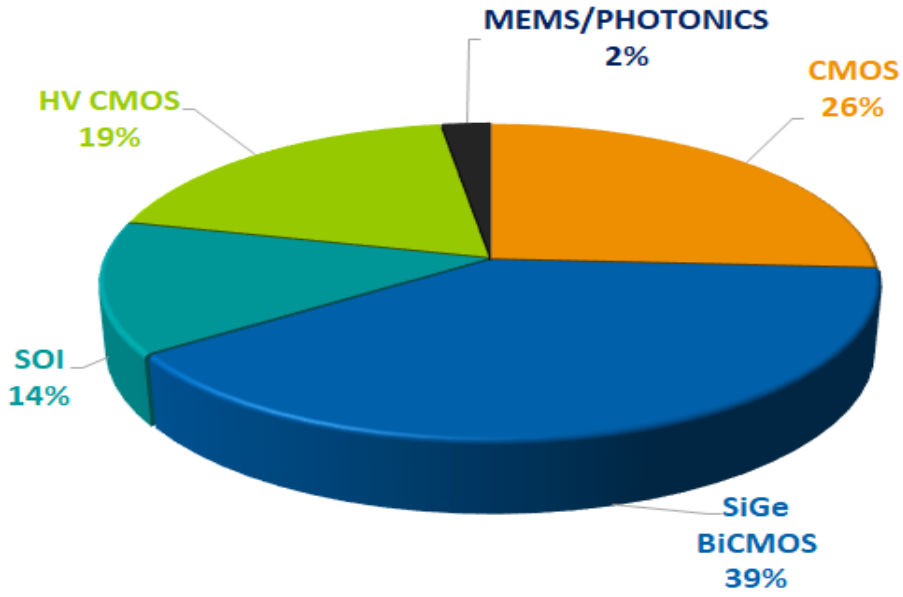
EUROPRACTICE IC SERVICE

Fraunhofer IIS · imec · UKRI Science and Technology Facilities Council · Tyndall National Institute

Activity in 2020





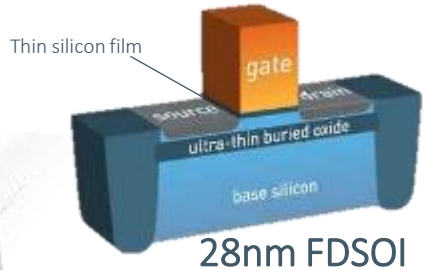


CMOS/BiCMOS/Advanced CMOS ICs

Long lasting success story of ams & STMicroelectronics advanced CMOS/BiCMOS MPW services

Manufacturing volumes through CMP:

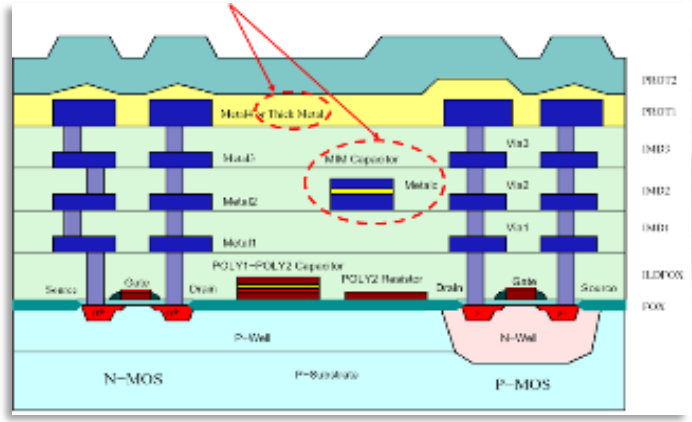
- ams: +4050 since 1992
- ST 130nm: +860 since 2003
- ST 65nm CMOS: +780 since 2006
- ST 28nmFDSOI: +360 since 2012
- ST 55nm SiGe: +140 since 2015



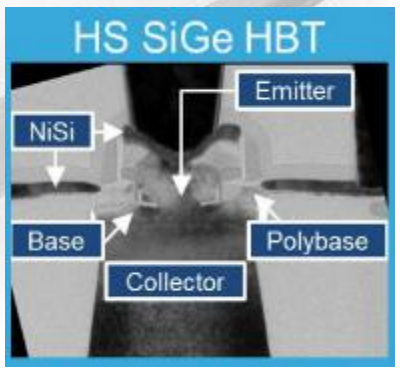
28nm FDSOI

CMOS 65nm
BiCMOS 55nm

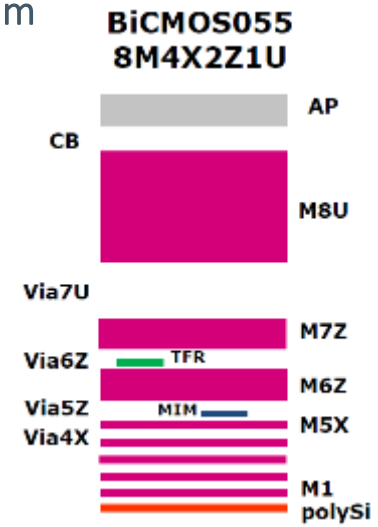
Thick Metal and MIM available in C35B4M3



0.35µm CMOS-RF process cross section



High speed SiGe HBT transistor
(courtesy of STMicroelectronics)



Design-Kit distribution

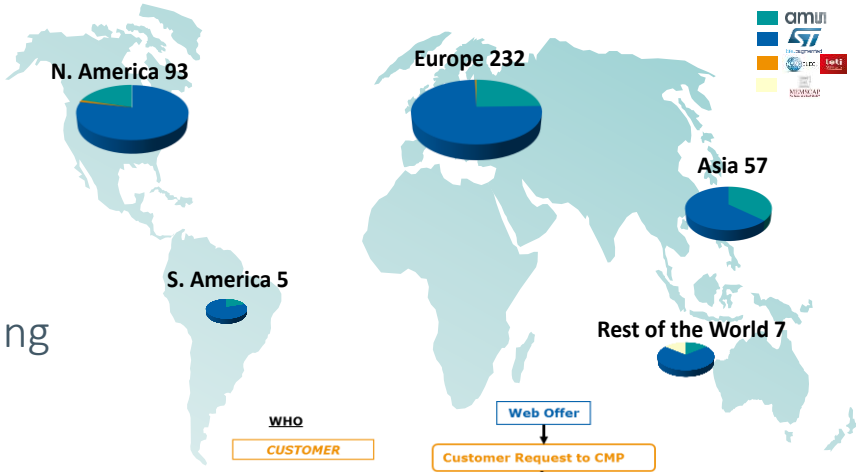
CMP distributes Design-Kits (DKs), containing technology files, models, and comprehensive set of standard cell libraries.

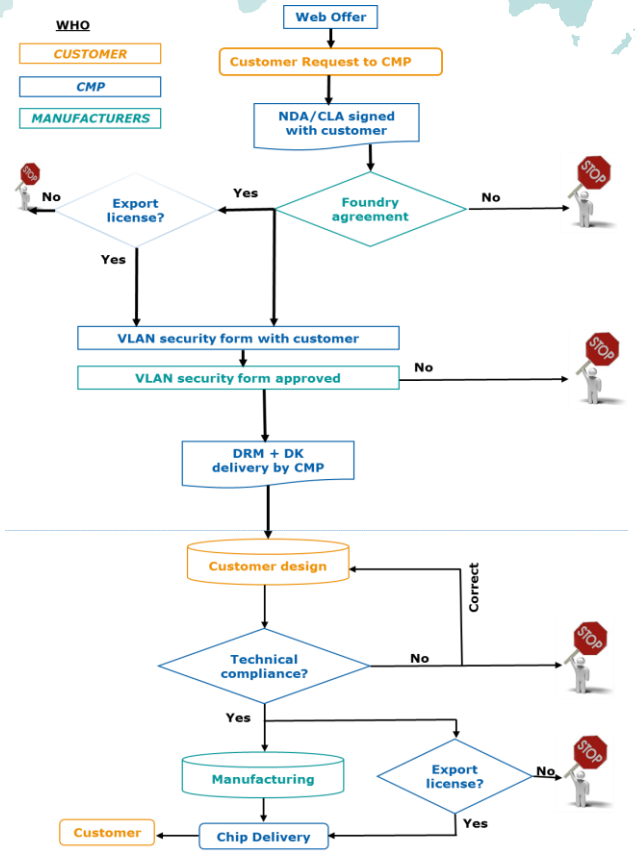
More than 40 different design-kits are supported by CMP, corresponding to IC's, Photonic IC's or MEM's technologies from different foundries.

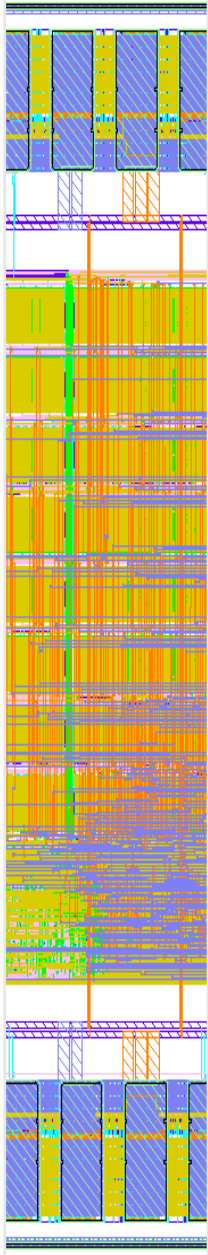
DKs are delivered after signature of a NDA/CLA and upon conditions that :

- **The provider agrees**
- **The designs are submitted to CMP for fabrication.**

- Users are updated with new versions when available.
- Technical support is provided through a HelpDesk
- Training are available for ST 28nm FDSOI aand 55nm SiGe
- Tutorials are provided as add-ons to Design-Kits.





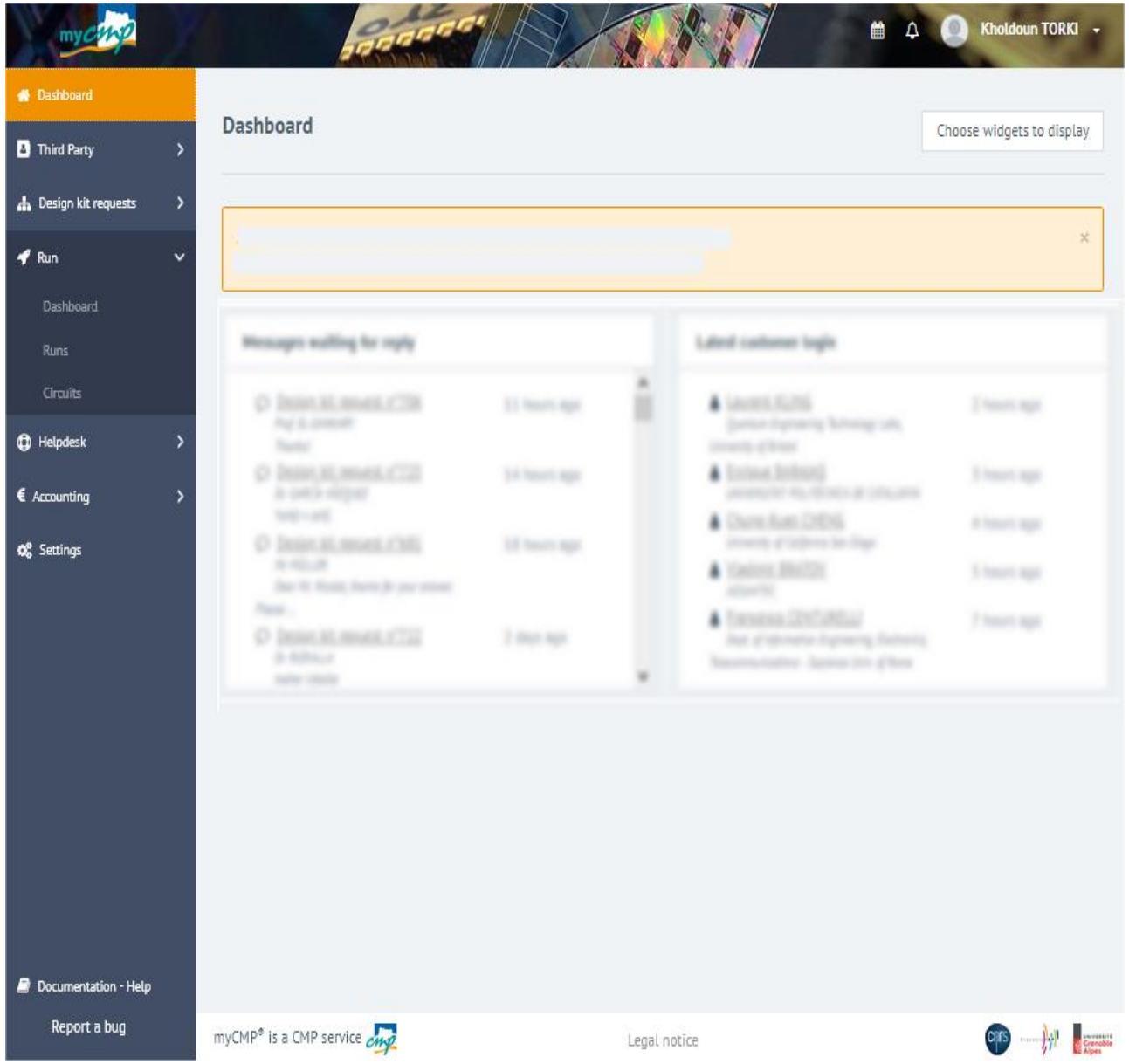


myCMP® CRM Web interface

All-In-One CRM Web Interface:

- Make DK Access Request
- Track Administrative Process
- Access to the HelpDesk & FAQ
- Tape-Out Submission

https://crm.mycmp.fr



Submission on Shuttle runs

CMP supports a wide portfolio of technology nodes, **with shuttles runs** available for each.

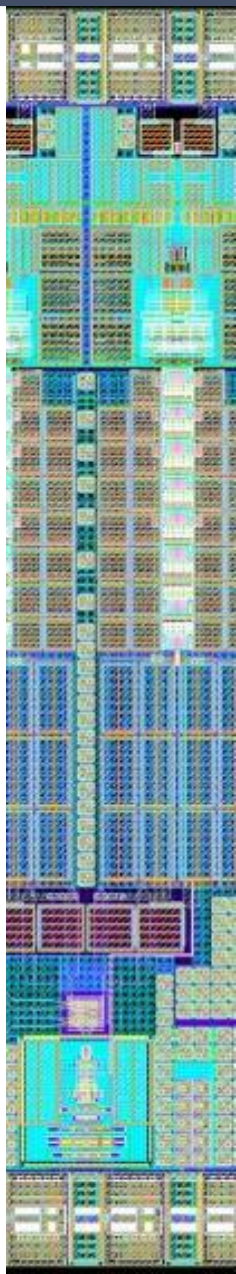
More than **70 runs** are planned in 2021

MPW run Calendar in 2021

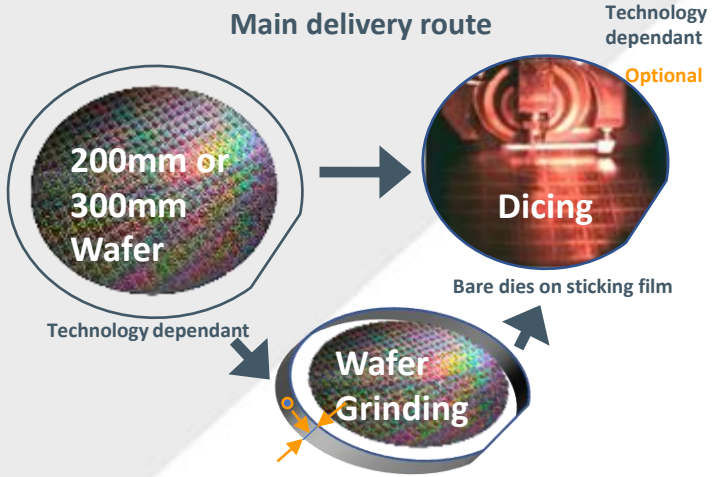
2015 | 2016 | 2017 | 2018 | 2019 | 2020 | **2021** | 2022

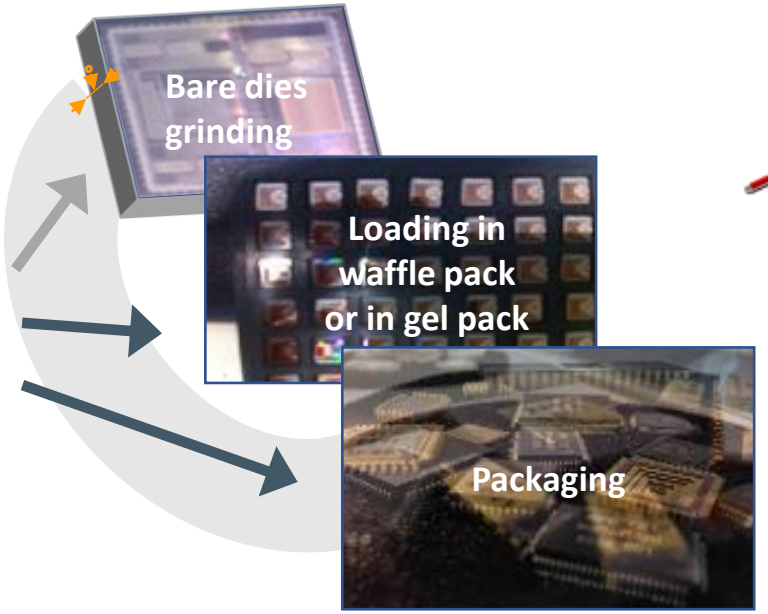
STMicroelectronics	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
IC 28nm CMOS28FDSOI			29						20			
IC 55nm BiCMOS055					31						2	
IC 65nm CMOS065					24						2	
IC 130nm BiCMOS9MW			1			7				29		
IC 0.16µm BCD8sP					21				17			
IC 0.16µm BCD8s-SOI				30								
ams	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
IC 0.35µm BARC C35B4OA		22				28				25		
IC 0.35µm C35B4C3		22				28				25		
IC 0.35µm ARC C35B4O1		22				28				25		
IC 0.35µm RF C35B4M3		2							27			
IC 0.35µm H35B4D3					3						8	
IC 0.35µm S35D4M5		2							27			
MEMSCAP	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
MEMS Specific MEMS technologies PolyMUMPs		16				17				19		
MEMS Specific MEMS technologies SOIMUMPs			2				9				2	
MEMS Specific MEMS technologies PiezoMUMPs	12				4			24				
IRT Nanoelec/CEA-LETI	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
Si-Photonics IC Si-220		15										1
Si-Photonics IC Si-310									6			
SiN-Photonics IC Si3N4-800				26								
ON Semiconductor	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
IC 0.18µm CMOS ONC18MS		1		6		7		9		11		6
IC 0.18µm CMOS HV ONC18-I4T		1		6		7		9		11		6
IC 0.35µm CMOS ONC35U	25			12			1		13			1
IC 0.35µm CMOS HV ONC35-I3T25U	25			12			1		13			1
IC 0.35µm CMOS HV ONC35-I3T50U			1		25				1			1
AMF	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
Si-Photonics IC SiP			22							25		
em microelectronic	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
IC 0.18µm CMOS EMALP018 logic		2				1				4		
Teem Photonics	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
Glass-photonics IC ioNext-NIR			22			21				25		
Glass-photonics IC ioNext-VIS			22			21				25		

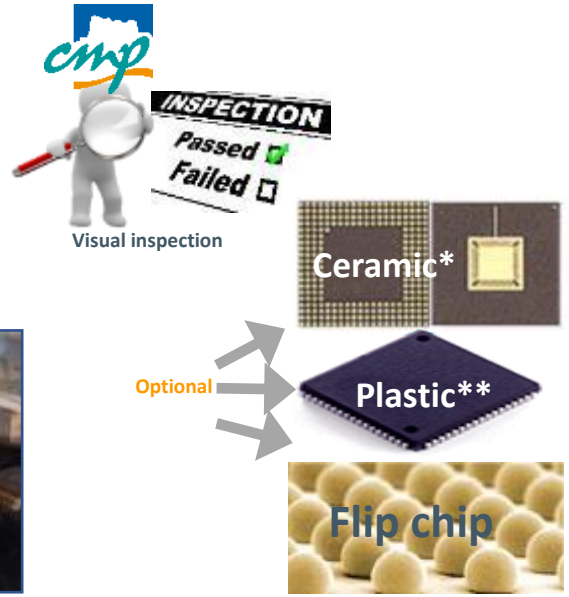
Notes:



Packaging Services



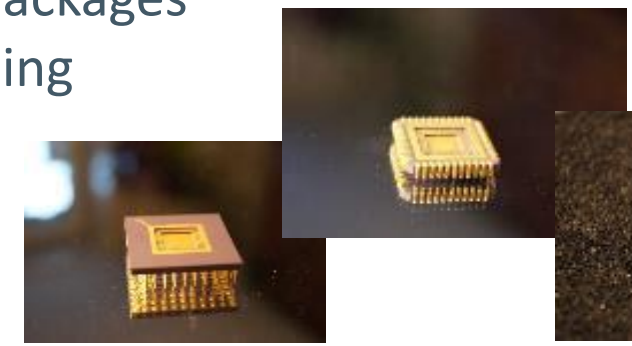


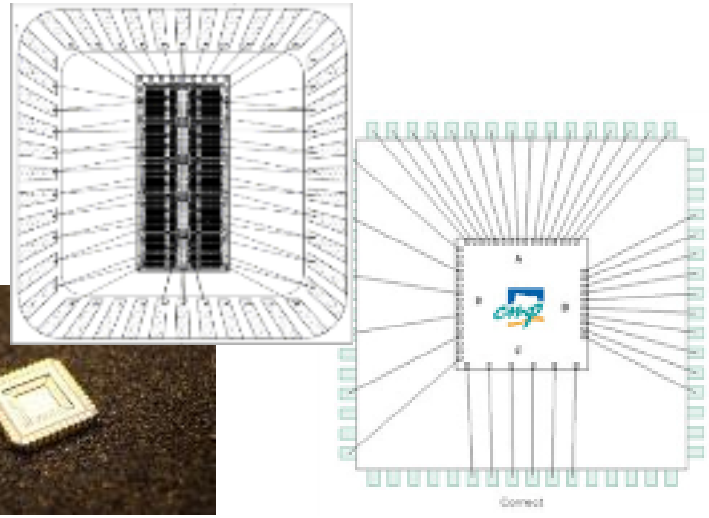


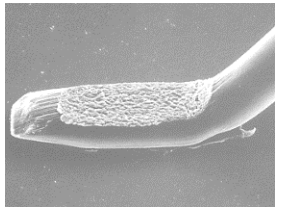
*Standard quantity from 5 to 25 pieces
**Recommended for >30 pieces.

Wire bonding

- Standard & custom packages
- Bonding diagram check & validation
- Ceramic & plastic packages
- Wedge & ball bonding





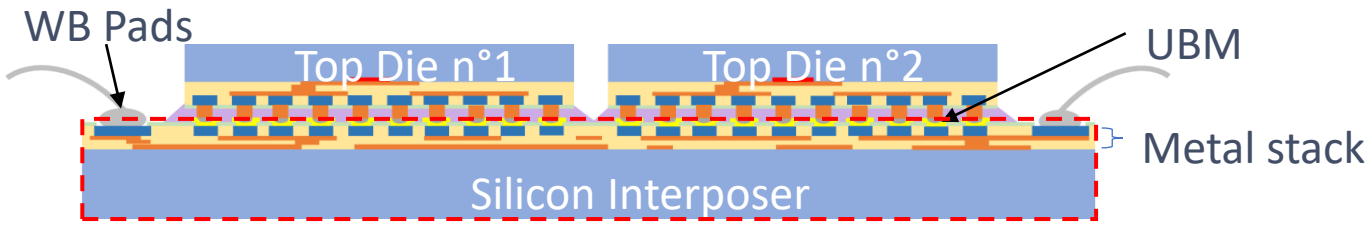


Advanced packaging

Silicon INTERPOSER MPWs on ams 0.35 µm 4 ML (3+1 Thick)

Active (Front & Backend) & Passive (Backend)

UBM deposited (Ni/Pd/Au)

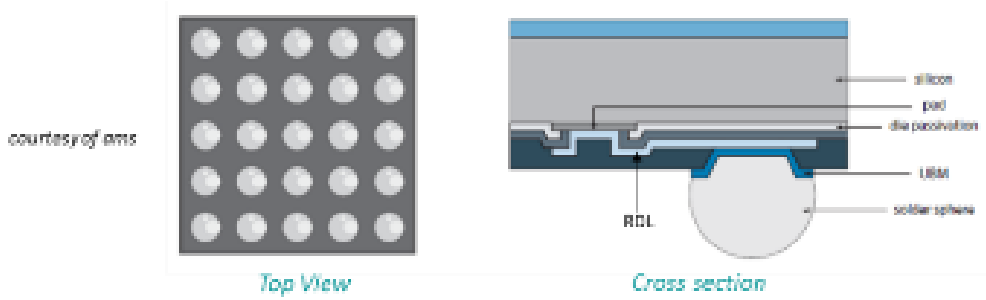


Wafer-level Bumping on any ams 0.35

Evenly distributed array over chip surface

Connections to CMOS pads with RDL layer

I/O Pitch compatible PCB assembly processes



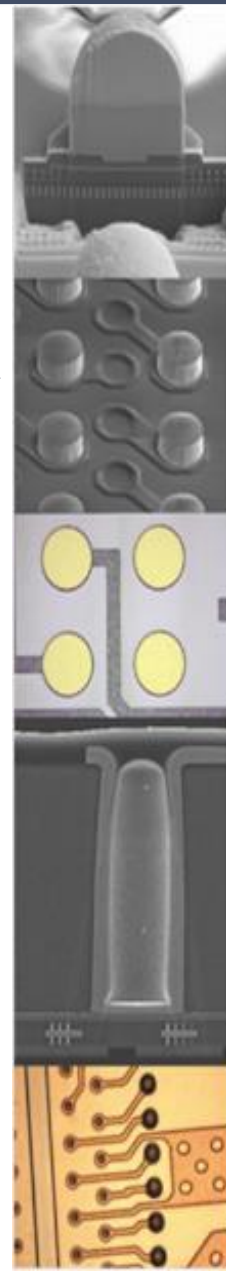
Wafer-level Bumping on MPW run in 300mm

Copper Pillar + Sn/Ag alloy capping

Small Diameter / Height: 62µm / 65 µm

Fine pitch (down to 90µm)

Courtesy STMicroelectronics



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