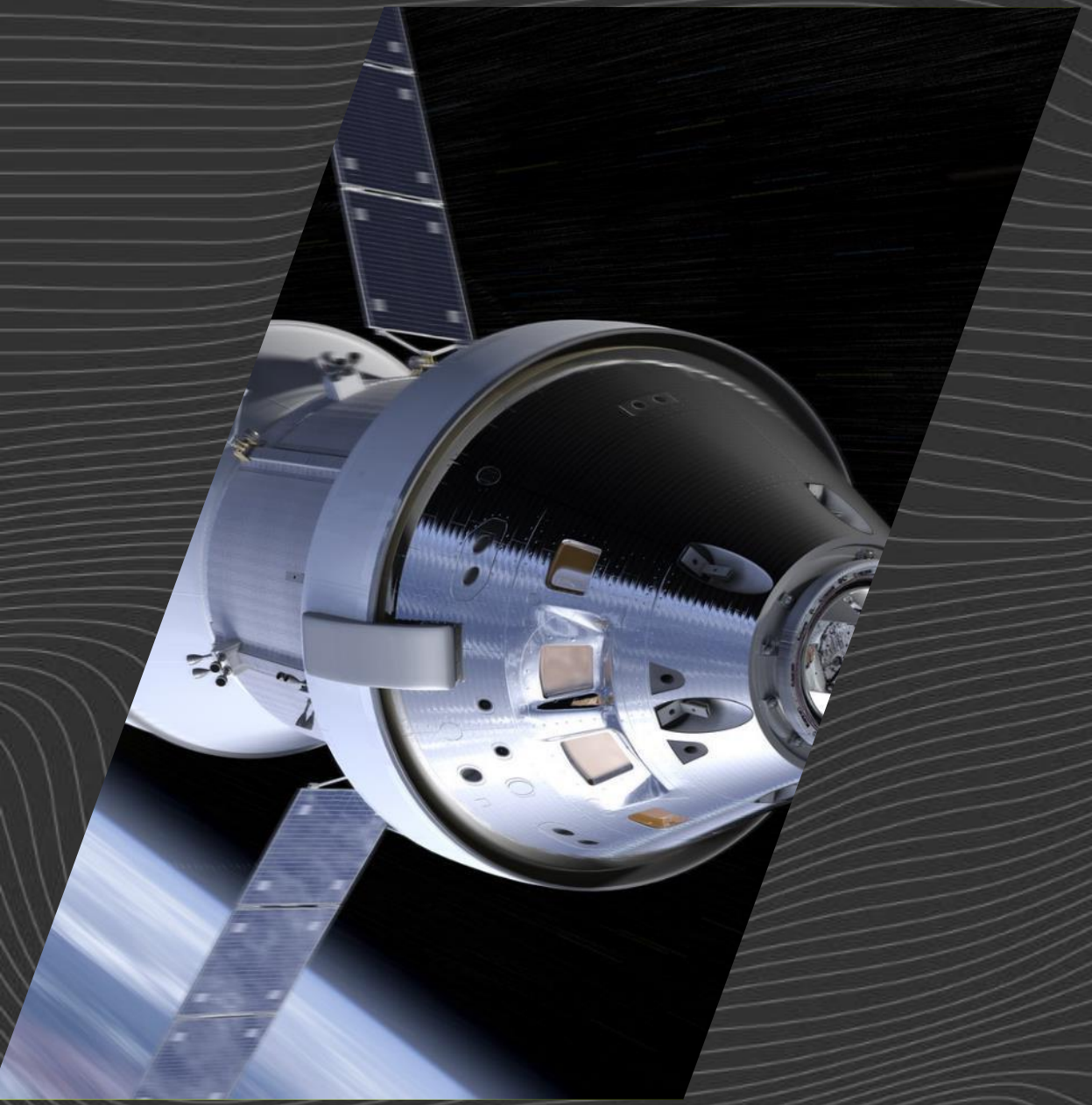

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# NOEL-V
## RISC-V Processor latest development roadmap and applications

3rd RISC-V Meeting

2021-03-30

# Agenda

- NOEL-V processor
- Development roadmap
- Hypervisor extension
- GR7xV

# NOEL-V processor

# NOEL-V Processor Core

## RISC-V RV64 and RV32 Processor Model

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**Characteristics:**

- RISC-V 32- and 64-bit compliant processor core
- **Superscalar – dual issue**
- Fault Tolerance - Error Correction Codes (ECC)
- **Leverage** foreseen uptake of **RISC-V software** and tool support in the commercial domain
- **Compatible with GRLIB IP Core library**

**Primary feature set:**

- **RISC-V RV64GC**
- AHB and AXI4 bus support

**Performance (currently):**

- CoreMark*/MHz
  - dual-issue 4.41**
  - single-issue 3.05**

https://www.gaisler.com/NOEL-V

* GCC9.3.0 20200312 (RTEMS 5, RSB 5 (c53866c98fb2), Newlib 7947581
-g -march=rv64ima -mabi=lp64 -B /gsl/data/products/noelv/rtems-noel-1.0.3//kernel/riscv-rtems5/noel64ima/lib --specs bsp_specs -qrtems -lrtemsdefaultconfig -O2 -funroll-all-loops -funswitch-loops -fgcse-after-reload -fpredictive-commoning -mtune=sifive-7-series -finline-functions -fipa-cp-clone -falign-functions=8 -falign-loops=8 -falign-jumps=8 --param max-inline-insns-auto=20

** Using "#define ee_u32 int32_t" in core_portme.h, as is common for 64 bit RISC-V.


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# NOEL-V Processor Architecture

**RISC-V RV64GC (IMAFDC):**

- 64/32-bit Base integer instructions (**RV64I or RV32I**)
- MUL/DIV (**M**)
- Atomics (**A**)
- Single/Double Float (**FD**)
- Compressed instructions (**C**)
- Supported modes: **M/S/U**
- MMU (**Sv39/Sv32**)
- Physical Memory Protection (**PMP**)

**Pipeline features:**

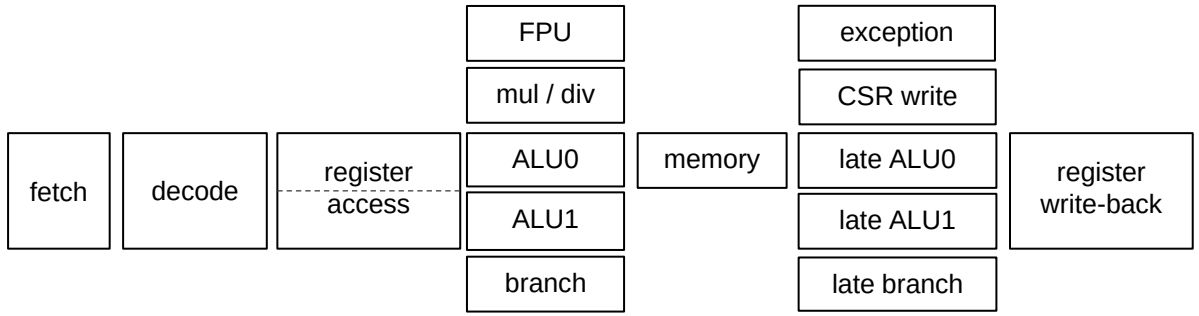
- 7-stage dual-issue in-order
- Late ALUs and branch unit
- Dynamic branch prediction
  - **BTB**, **BHT**
- Return Address Stack (**RAS**)

**Additional extensions:**

- Hardware hypervisor support (**H**): Being implemented
- Bit Manipulation (**B**): Pending standardization
- User-level interrupts (**N**): Pending standardization
- Vector operations (**V**): Being investigated

**L1 cache:**

- Separate instruction and data caches
- Up to 2x16 kByte
- Up to 4-way associativity
- Single cycle access



# NOEL-V Configurations

- The NOEL-V processor core is available as part of a subsystem that also contains system peripherals. The subsystem can be configured to use the processor configurations listed in the table below.

| Configuration | ISA | Pipeline | Cache | MMU | PMP | FPU | Note |
|---|---|---|---|---|---|---|---|
| **TIN32** | RV32IM | single issue | no | no | no | no | Tiny configuration |
| **MIN32** | RV32IMAC | single issue | yes | no | yes | no | Minimal 32-bit configuration |
| **MIN64** | RV64IMAC | single issue | yes | no | yes | no | Minimal 64-bit configuration |
| **GPP32** | RV32GCH | single issue or dual issue | yes | yes | yes | GRFPU or NanoFPU | General purpose 32-bit configuration |
| **GPP64** | RV64GCH | single issue or dual issue | yes | yes | yes | GRFPU or NanoFPU | General purpose 64-bit configuration |
| **HPP32** | RV32GCH | dual issue | yes | yes | yes | GRFPU or NanoFPU | High-performance 32-bit configuration, primarily targeting ASIC |
| **HPP64** | RV64GCH | dual issue | yes | yes | yes | GRFPU or NanoFPU | High-performance 64-bit configuration, primarily targeting ASIC |

- It is also possible to tailor additional configuration settings to create custom processor configurations by editing the VHDL generic (configuration parameter) assignments in the subsystem.
- Maximum operating frequency is continuously improved on all different platforms from FPGAs to ASIC technologies.
- Please see https://www.gaisler.com/NOEL-V for latest version and updates

# NOEL-V Processor Peripherals

**RISC-V Debug Module (DM)**

- Compatible with the RISC-V debug specification
- JTAG Debug Module Interface
- Hart Run Control
- GPR and CSR register access
- Program buffer
- Triggers (match and instruction count)

**RISC-V Platform Level Interrupt Controller (PLIC)**

- Compatible with the Platform Level Interrupt controller specification

**Also complemented by**

- New DDR2 and DDR3 SDRAM controller (FTADDR23), specifically targeted for space applications
- Multi-port L2 cache extensions allowing bandwidth extensions from L1 to off-chip memory devices

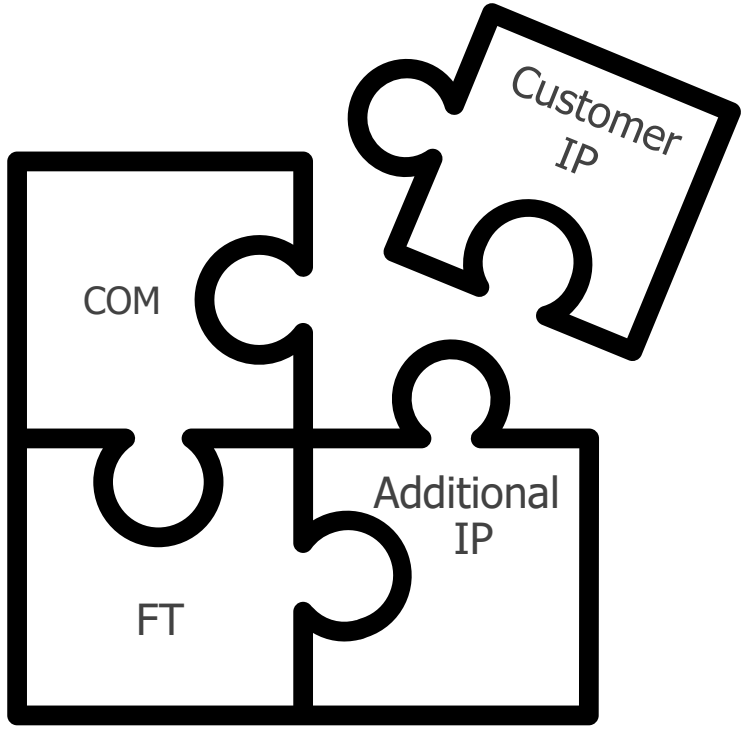
**L2 cache** (commercial license)

- AHB or AXI4 back-end
- Up to 128 bit wide frontside and back-end
- LRU or pseudo-random
- Up to 4-way associativity and 2 Mbyte
  - Can be split between cores
- Address range configurable
  - Write-through
  - Write-back
  - Uncacheable

# IP-Core licensing model

**Commercial licensing**

- Three groups of IP-Cores:
  - COM- standard distribution
  - FT – Standard with fault tolerant features
  - Additional IP-Cores
- Enables proprietary designs
- Covered by support agreement GRLIB [www.gaisler.com/getgrlib](www.gaisler.com/getgrlib)




**Free open source, GNU GPL**

- Limited number of IP-Cores
- Enables evaluation before decision
- Extensively used by academia and hobbyists
- Not for commercial designs
- GRLIB community

GPL

Free open source

GRLIB community

# Development roadmap

# Development roadmap

**Next release (V5, July 2021)**

- H extension (Hypervisor support)
- C extension (Compressed instruction support)
- Support for GRFPU (high-performance FPU)
- FT support (fault-tolerance)

**Future releases**

- Multi-port bus connection between processor core and L2 cache
- TCM (tightly coupled memory)
- Zbb extension (Bit manipulation)

**Feature to be evaluated**

- CMO support (Cache Management)
- P and V extensions (Vector support)
- Support for more resource efficient floating-point implementations
- N extension (User mode interrupts)
- Core-Local Interrupt Controller (CLIC)
- Additional subset(s) of B extension

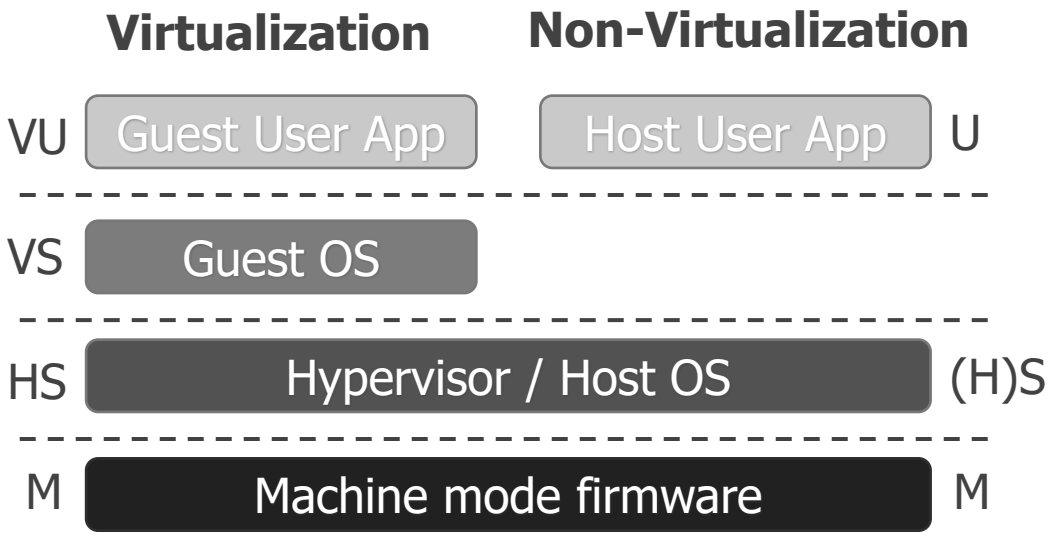
# Hypervisor extension

# Hypervisor extension

## Implementation ongoing

**Implementation**

- Targeting current draft (0.6.1)
- **S-**mode transformed into **HS**-mode
- Added virtualization modes **VS** and **VU**
- Added new CSRs
  - Hypervisor CSRs (**h..**)
  - Virtual Supervisor CSRs (**vs...**)
  - Machine CSRs (**mtval2**, **minst**)
- Updated machine mode CSRs
  - **mstatus**, **mideleg**, **...**



# Hypervisor extension

## Implementation ongoing

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**Hypervisor interrupts**

- Guest external interrupts (CSRs **hgeip** and **hgeie**)
- Support *direct assignment* of interrupt to virtual machines
- Number of PLIC context associated with a hart is extended.

**MMU update**

- Currently only support for RV64 Sv39x4
- Two-stage address translation
  - Hardware page table walk
  - Guest physical TLB (second-stage)
  - First-stage TLBs include complete address translation

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# Hypervisor extension

## Verification ongoing

**Direct tests**

- CSRs
- Hypervisor instructions
- Two-stage address translation
- Interrupts
- …

**Random tests**

- Update random generator
- Utilize virtualization mode
- Hypervisor instruction
- Two-stage address translation

**Hypervisors**

- Xvisor
- XtratuM
- Jailhouse

**Reference implementations**

- Spike
- QEMU

# GR7xV

16-core NOEL-V Processor

# Funded EU projects for RISC-V developments

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De-RISC

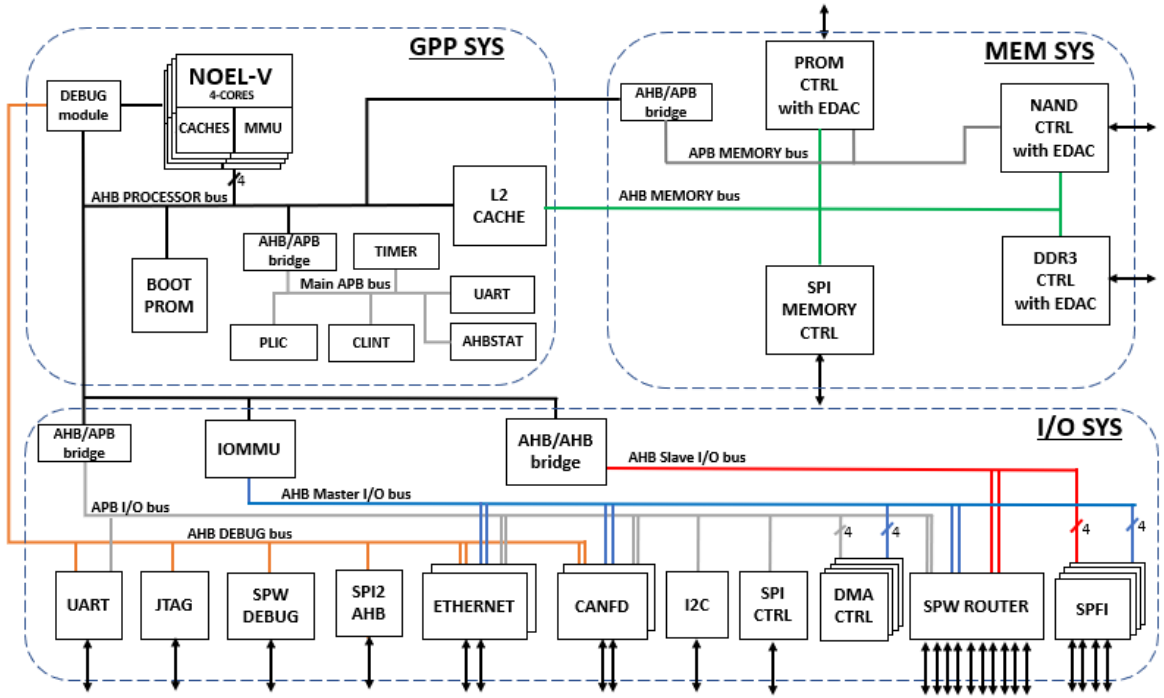
Dependable Real-time Infrastructure for Safety-critical Computer

- Main output: Stack consisting of development board, NOEL-V SoC, XtratuM hypervisor
- Consortium: Thales Research & Technology, FentISS, Barcelona Supercomputing Center

SELENE

Self-monitored Dependable platform for High-Performance Safety-Critical Systems

- Main output
  - NOEL-V feature development
  - RISC-V multicore platform
- Consortium: Universities and industry companies




The project enables development of GR7xV SoC building blocks and creates new alliances

RISC-V

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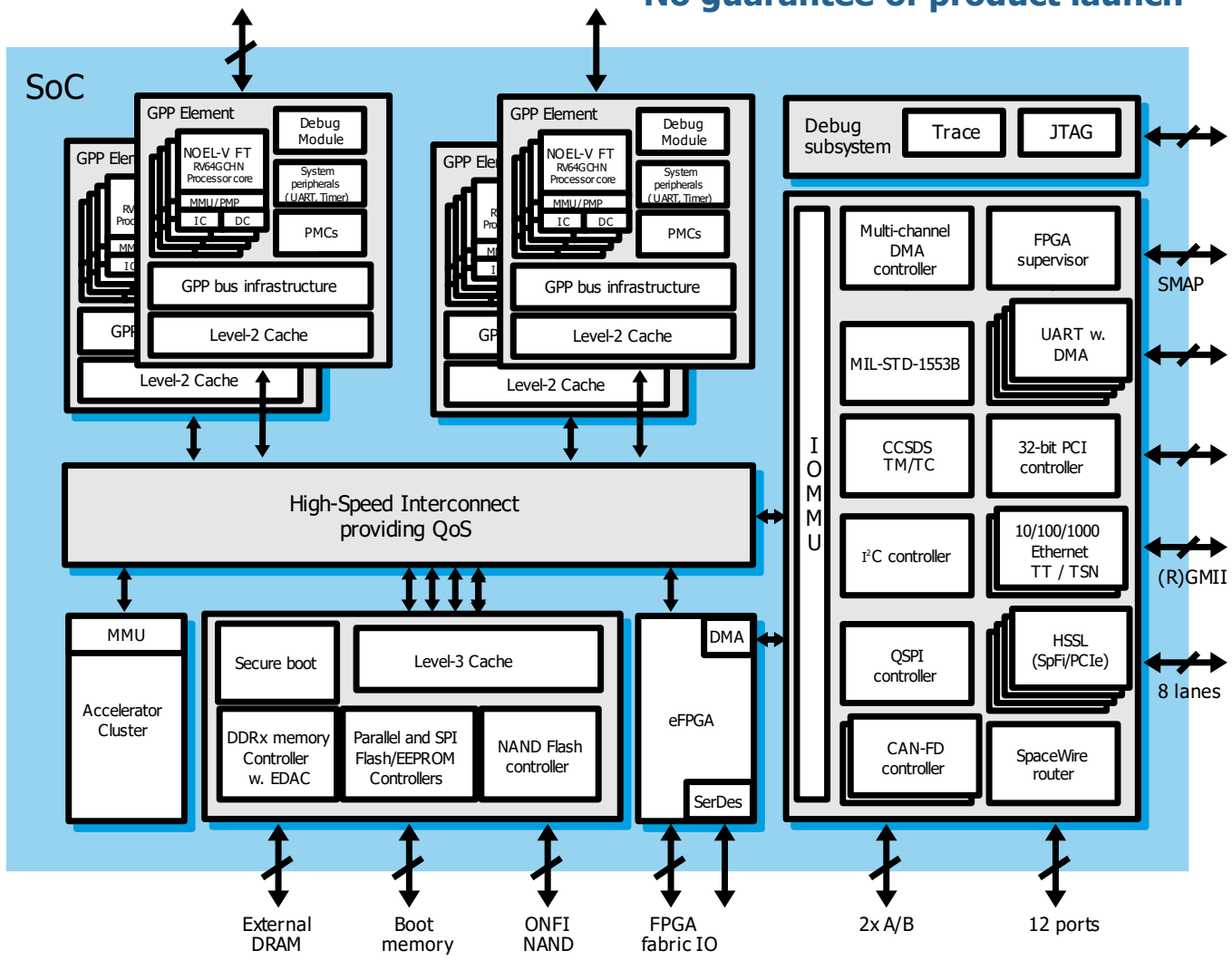
European Commission

# GR7xV – 16-core NOEL-V Processor

**In development**
**No guarantee of product launch**

**Baseline Features**

- Fault Tolerant 64-bit RISC-V Hexadeca-core with islands of 4 general-purpose processors each with dedicated L2 Caches
- Accelerators for high-performance computation
- Performance targets:
  - GPP: 19.2 GOPS, 9.6 GFLOPS, 7700 DMIPS – 31000 DMIPS
  - Accelerator: 1.23 TOPS of INT8.32 for MDL, 19 GFLOPS FP16, 8.5 GFLOPS FP32
  - TID: target 100 krad(Si)
- DDR2/3/4 SDRAM memory I/F (w. EDAC)
- JESD204B/C support TBD
- CCSDS TM/TC functions on-chip
- Increased focus on cyber-security and isolation (processor and SoC design features)
- Software support effort on the way: XtratuM support provided before component launch
- First available in plastic package, ceramic later
- Target technology: GF 22 FDX

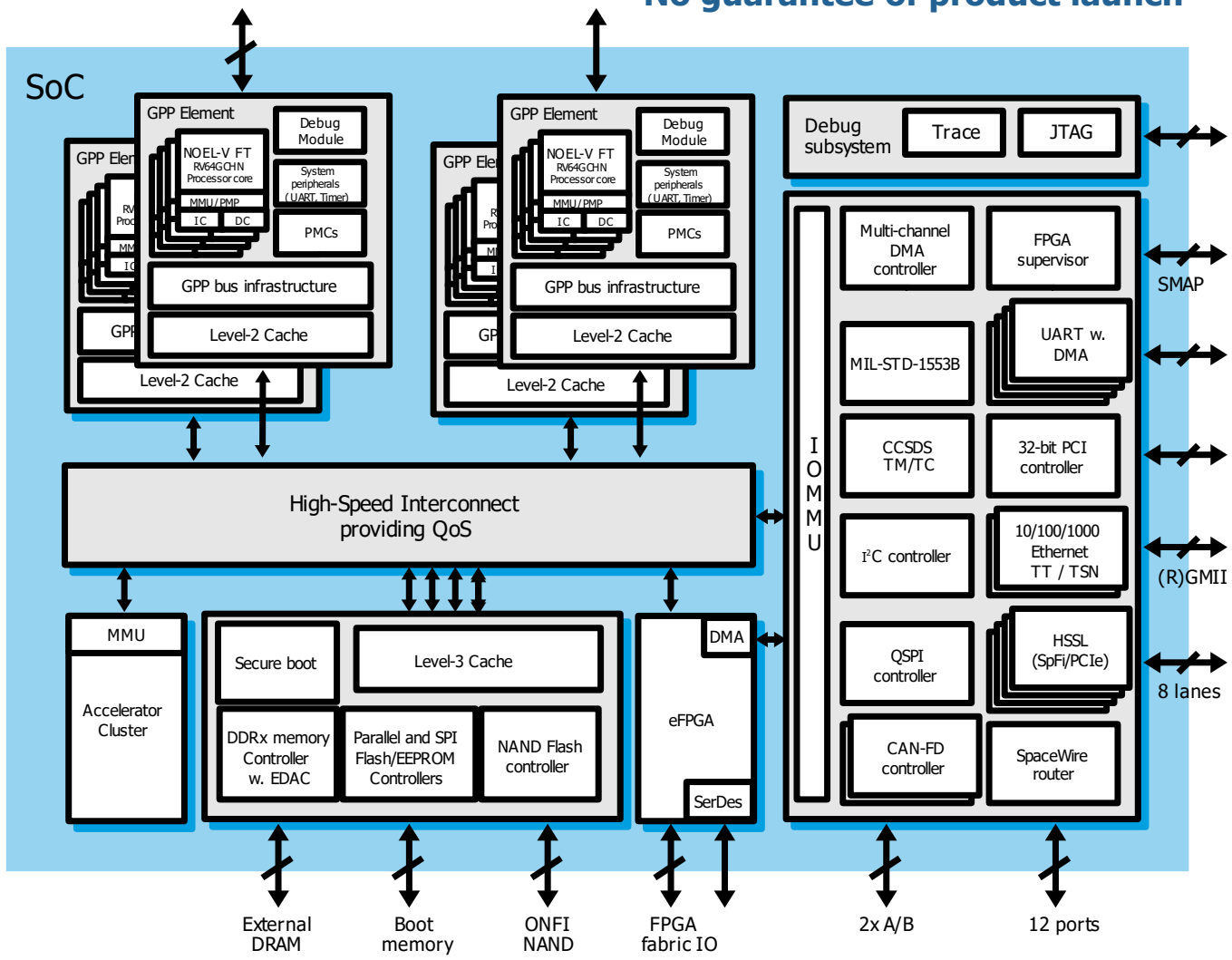


# GR7xV – 16-core NOEL-V Processor

**In development**
**No guarantee of product launch**

**Baseline Interfaces**

- SpaceFibre, PCIe, 8 lanes 6.25 Gbit/s
- 12-port SpaceWire router with +4 internal port
- 32-bit 33 MHz PCI interface (TBD)
- 2x 10/100/1000 Mbit Ethernet
- MIL-STD-1553B
- CAN-FD
- 8 x UART with DMA, SPI master/slave, Timers & Watchdog GPIO
- $I^2C$ master/slave
- NAND Flash controller interface
- Interfaces for connecting COTS accelerators TBD
- Debug links: Ethernet, JTAG, SpaceWire



# NOEL-V release

- NOEL-V is available as part of the GRLIB IP Library
- GRLIB contains a wide range of peripheral IP cores and provides template designs for several FPGA boards, including Xilinx KCU105, Xilinx VC707, Microchip PolarFire Splash Kit, and Digilent Arty A7
- NOEL-V is a highly configurable RISC-V 64/32-bit processor IP core. Several standard configurations have been defined and are listed at www.gaisler.com/NOEL-V
- Prebuilt bitstreams are available for the Xilinx KCU105 board (www.gaisler.com/NOEL-XCKU), Digilent Arty-A7 (www.gaisler.com/NOEL-ARTYA7), and the Microchip PolarFire Splash Kit (www.gaisler.com/NOEL-PF)
- The 2020-December release of the NOEL-V RISC-V processor includes configuration options ranging from the High-Performance 64-bit RV64G (HPP64) to our tiniest 32-bit RV32IM (TIN32).
  - B, C, H, N and V extensions not yet supported by open source release
  - Free open-source model does not include fault-tolerance features
  - In the July 2021 C and H extension will be released
- Logic utilization results are available in area spreadsheet available at www.gaisler.com/getgrlib


www.gaisler.com/NOEL-V
www.gaisler.com/getgrlib
grlib.community

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