Solving your on-chip processing challenges

Codasip Solutions

codasip
RISC-V PROCESSORS

Selection of processors for many applications

- Low power & high performance embedded
- Application processors
- RISC-V-compliant
- Configurable

Modify Codasip RISC-V Processors using Codasip Studio

- Add custom instructions to accelerate your algorithms
- Use existing design as a base of your processor

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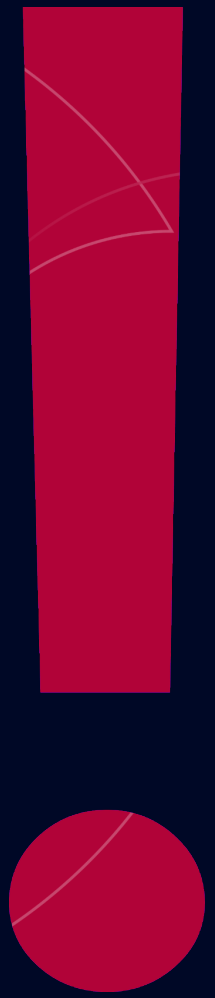
STUDIO

Create processors using a high-level description

- Fine-tune the design for performance, area and power
- Automatically generate software and hardware development kits

Select and / or Modify



The Off-The-Shelf Processor Portfolio

Available **immediately**

Pre-verified, **tape-out quality IP**

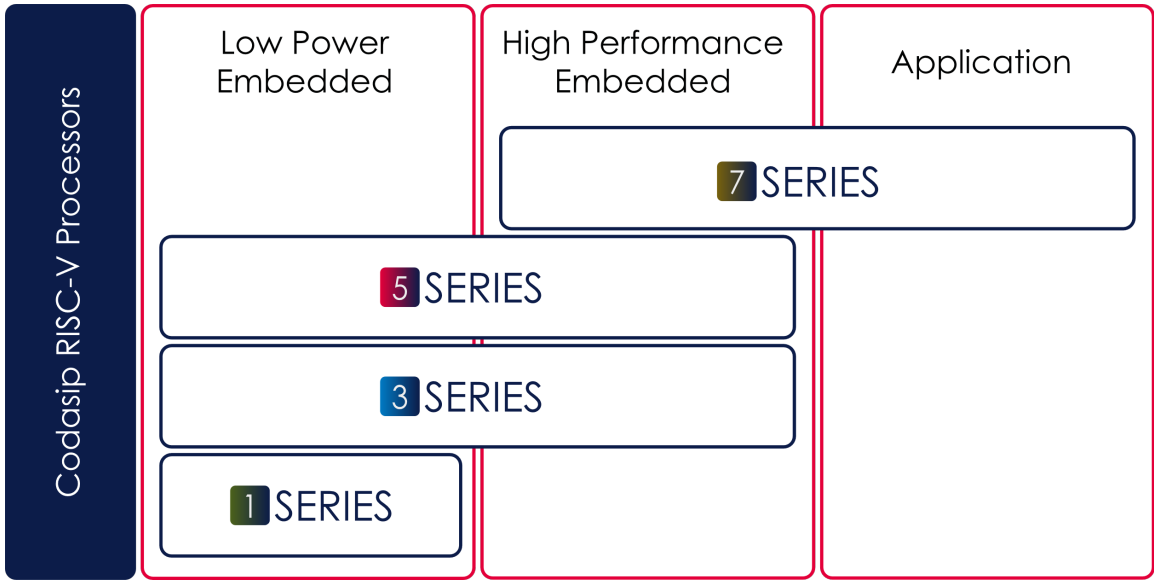
- Customers do not need to verify IP

All Codasip Processors are **RISC-V compliant**

- Implement RISC-V privilege specification
- Implement RISC-V debug specification

Industry-standard interfaces

- AMBA for instruction and data bus
- JTAG (4pin/2pin) for debugging



DSP Cores Under Development

Digital signal processing applications with **higher performance** and **lower power consumption**

Ideal for:

- Audio encoding/decoding
- Computer vision
- Sensor fusion

Enabled via **standard RISC-V P extension**

- SIMD operations
- Works on the integer register file
- Contains approximately 350 instructions

Early access to P extension in 7 series will be **available in Q1 2021**

Codasip RISC-V Processors	Low Power Embedded	High Performance Embedded	Application
7 SERIES			
5 SERIES			
3 SERIES			
1 SERIES			

Multiprocessor Available Soon

1-4 A70X processors in the cluster

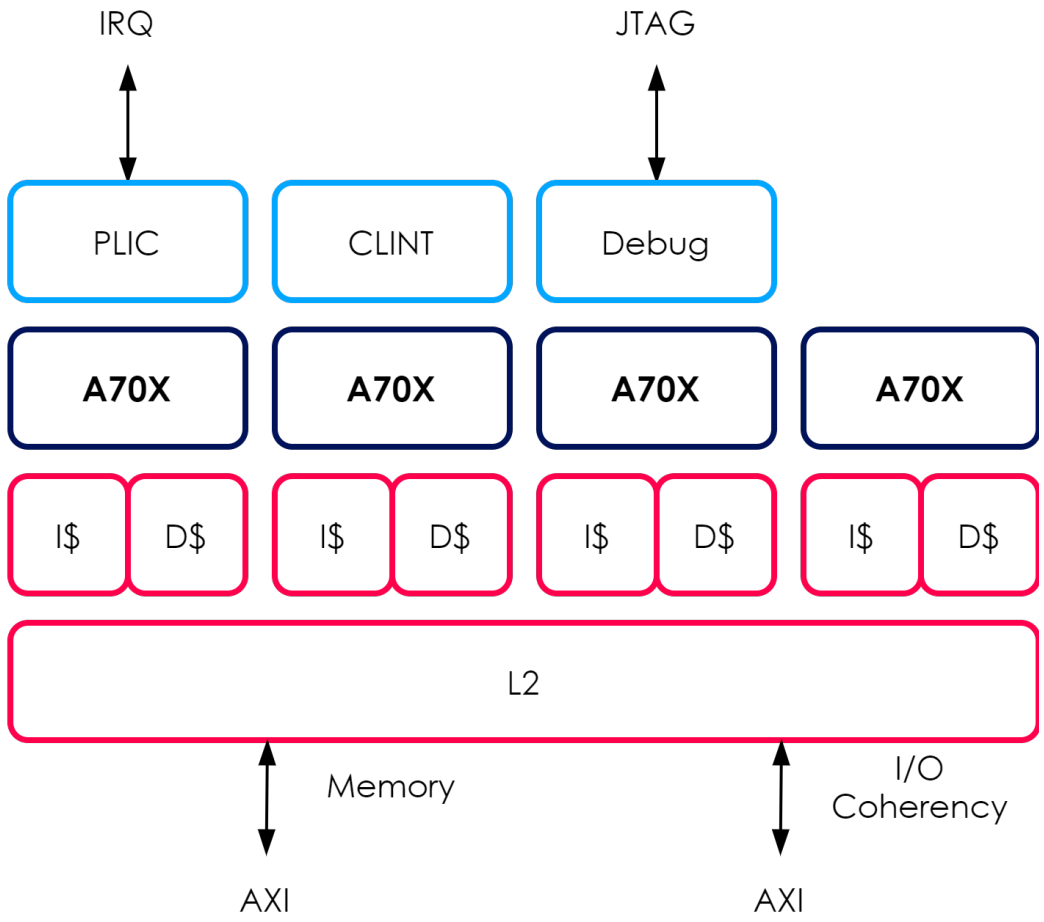
Coherent L1 and L2 cache

- L2 cache is also configurable
- AXI/CHI protocol on the L2 cache

Standard RISC-V interrupt controllers

- **CLINT** (core-level)
- **PLIC** (platform-level)

Early access **available in Q1 2021**



Software Development Kit

LLVM based compilation toolchain

- Includes compiler, assembler, disassembler and linker
- Newlib C/C++ standard libraries
- Proprietary optimizations by Codasip
- Outperforms community alternatives across a wide range of benchmarks

High-performance simulators

- Instruction set simulator
- Cycle accurate simulator

Debugger and profiler

- Simulator based debugger
- On-chip debugger

Codasip CodeSpace™

- Eclipse based IDE
- More explained later

Codasip FPGA Evaluation Platform

Processor subsystem running **RTOS or Linux**

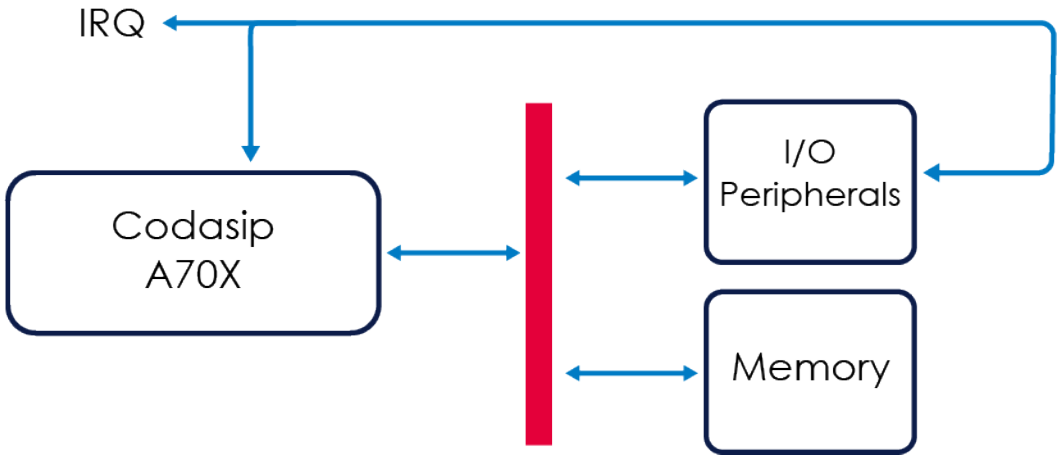
- Easily evaluate Codasip RISC-V Processors
- Port your software to RISC-V

Recommended **FPGA platform settings**

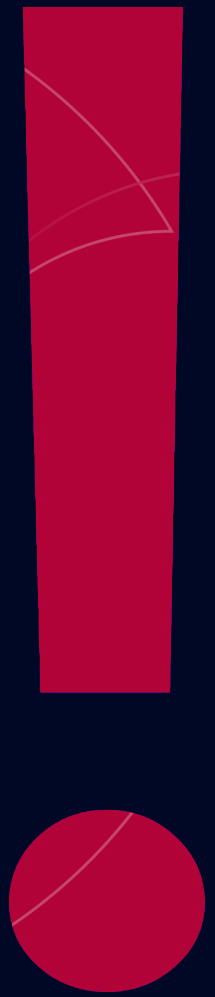
- Digilent Nexys-A7-100T FPGA board
- Digilent JTAG-HS2 Programming Cable
  - Alternatively Segger and IAR cables can be used

Up and running in **less than 15 minutes**

Step by step quick start guide for the recommended FPGA board



Modify and / or Create



What is Codasip Studio?

A unique collection of tools for **fast & easy modification** of RISC-V processors.
All-in-one, highly automated. Introduced in 2014, **silicon-proven** by major vendors.

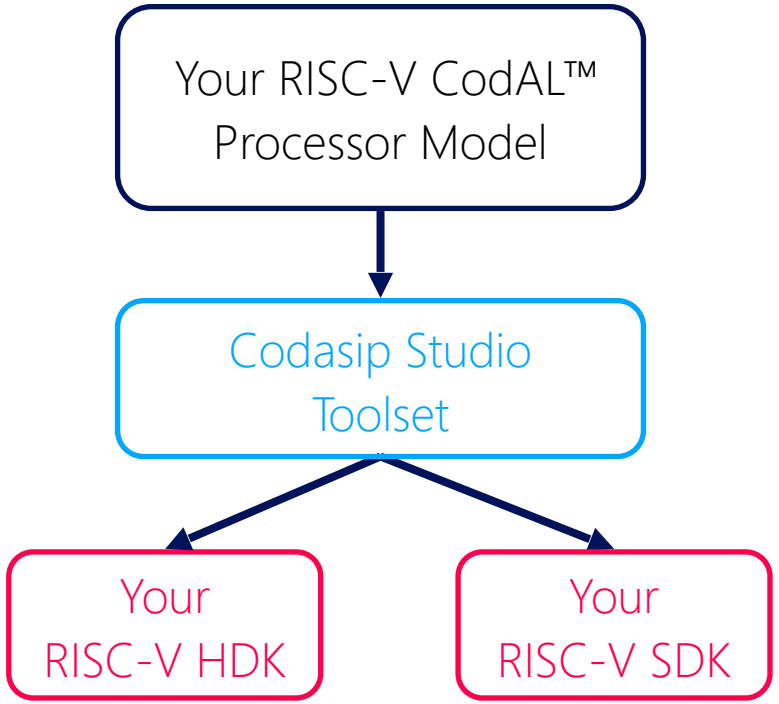
Processor described in **high-level** architecture description language

Allows customization of:

- Instruction set architecture (ISA)
- Micro-architecture

Users may choose to:

- **Modify** an existing Codasip RISC-V Processor
- **Design** new processor from scratch



Generated HDK and SDK

Hardware Development Kit (HDK)

- RTL (Verilog/VHDL/SystemVerilog)
  - Human readable
  - Links back to source CodAL
- SystemVerilog UVM test environment
- Integration test bench
- Sample EDA scripts
- SystemC co-simulation model

Software Development Kit (SDK)

- C/C++ LLVM compiler (improved by Codasip)
- C/C++ Libraries (newlib)
- Assembler, disassembler, linker
- High-performance instruction set and cycle accurate simulators
- Debugger and profiler
- Documentation and ISA visualization
- Random programs used during verification

CodAL™

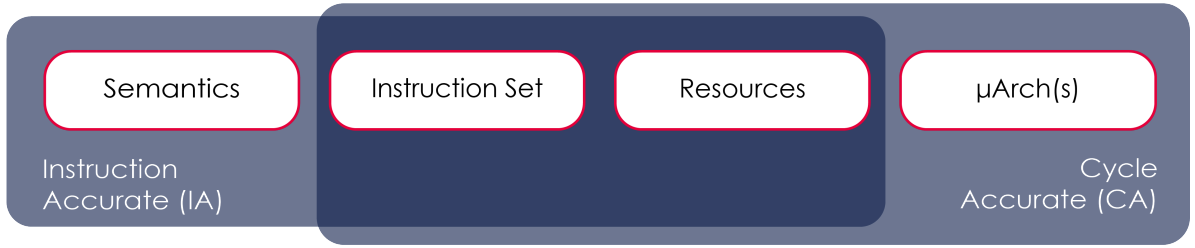
Easy-to-understand **C-like language** that models a rich set of processor capabilities

All Codasip processors are created and verified using CodAL

Multiple microarchitectures can be implemented in a single CodAL model

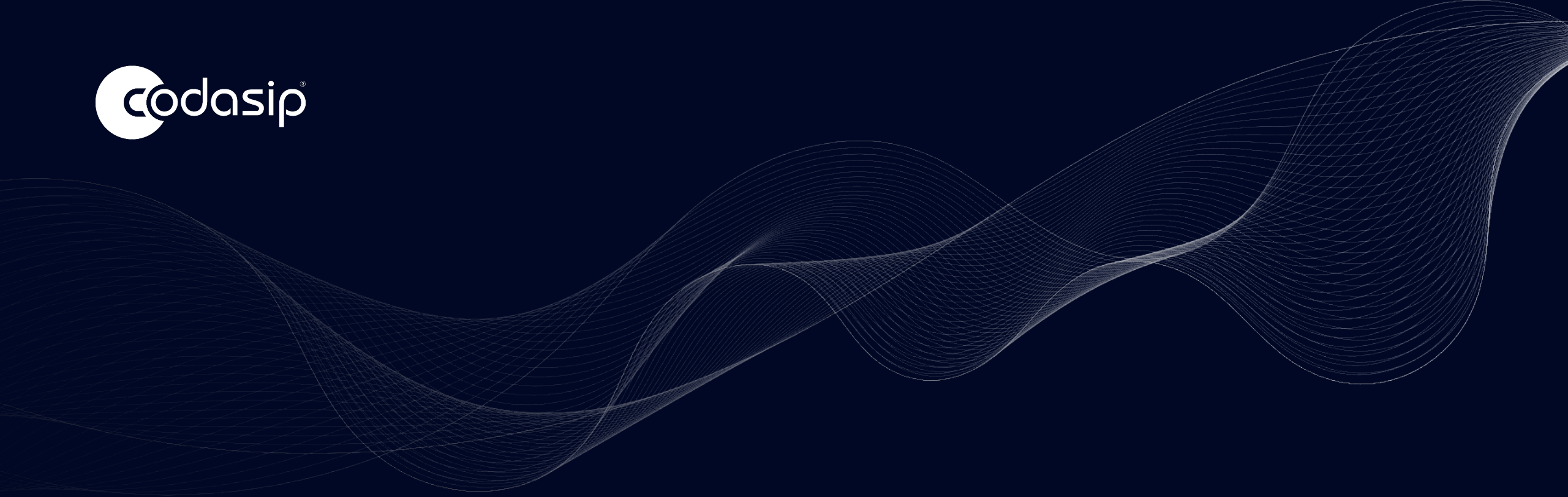
CodAL models are provided to Codasip IP customers as **a starting point** for their processor optimizations and modifications

CodAL Description




```
/*    Multiply and accumulate: semantics
                  dst += src1 * src2
*/

element i_mac {
          use reg as dst, src1, src2;
          assembler { “mac” dst “,” src1 “,” src2 };
          binary { OP_MAC:8 dst src1 src2 0:9 };
          semantics {
                    rf[dst] += rf[src1] * rf[src2];
          };
};
```



Now, it's your turn!

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