Open-Source RISC-V Cores

for use in high volume production SoCs

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www.openhwgroup.org

- OpenHW Group is a not-for-profit, global organization driven by its members and individual contributors where HW and SW designers collaborate in the development of open-source cores, related IP, tools and SW such as the CORE-V Family of open-source RISC-V cores

  - International footprint with developers in North America, Europe and Asia
  - Providing an infrastructure for hosting high quality open-source HW developments in line with industry best practices
  - Strong support from industry, academia and individual contributors worldwide

Industry Ecosystem
64+ Members & Partners

OPENHW GROUP™
PROVEN PROCESSOR IP

CORE-V™

Alibaba Group 阿里巴巴集团

bluespec

BSC Barcelona Supercomputing Center
Centro Nacional de Supercomputación

cea

FUTUREWEI Technologies

Imagination

NXP

SILICON LABS

VeriSilicon

AB Open

ALDEC THE DESIGN VERIFICATION COMPANY

aLean-Tec adding value to open source HW

AMIQ EDA

ASHLING

axiomise predictable formal verification

beagleboard.org

BTA DESIGN SERVICES your project, our team

CIRCUIT SUTRA TECHNOLOGIES

codeplay

DATUM

ECSPEC

em microelectronic

EMBECOSM®

GF®

GREENWAVES TECHNOLOGIES

HENSOLDT Detect and Protect

HUAWEI

IAR SYSTEMS

imperas

INTRINSIX

metrics

NEC

NVIDIA

onespin

> OPERSYS

PlatformIO labs

QuickLogic®

SECURE THINGZ

THALES

YosysHQ

Research Ecosystem
64+ Members & Partners

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

POLYTECHNIQUE MONTRÉAL
WORLD-CLASS ENGINEERING

Partner Ecosystem
64+ Members & Partners

Accounting, Legal, Banking

OpenHW Group Board of Directors

- Xiaoning Qi, Alibaba Group
- John Davis, Barcelona Supercomputing Center
- Charlie Hauck, Bluespec (Treasurer)
- Fabien Clermidy, CEA
- Liang Peng, Futurewei Technologies
- Tim Whitfield, Imagination Technologies
- Rob Oshana, NXP (Chairman)
- Alessandro Piovaccari, Silicon Labs
- Wayne Dai, VeriSilicon
- Rick O'Connor, OpenHW Group

Working Groups & Task Groups

- Board approves member-elected Chairs of ad-hoc working groups and has final approval of working group recommendations
  - Technical Working Group and Marketing Working Group are standing working groups
- Technical Working Group
  - Cores Task Group
  - Verification Task Group
  - SW Task Group
  - HW Task Group
- Marketing Working Group
  - University Outreach Task Group
- Together with internal OpenHW Group engineering staff, member company development engineers (FTEs / ACs) establish and execute OpenHW Group projects
  - 10 active projects across CORE-V RTL, Verification, GCC / LLVM, IDE, RTOS, FPGA, SoC, etc. with more projects in the pipeline

Technical Working Group (TWG)

- Co-Chairs
  - Sebastian Ahmed, Silicon Laboratories
  - Jerry Zeng, NXP Semiconductors
- Drive the overall technical direction, development roadmap and project execution for all technology related activities within the OpenHW Group and oversee the Task Groups
  - TWG is essentially the OpenHW Group company's "R&D / Engineering Organization"
- OpenHW Group engineering release methodology is based on the Eclipse Development Process
  - All OpenHW Group Platinum / Gold / Silver members are also Solutions members of the Eclipse Foundation

Cores Task Group

- Chair: Arjan Bink, Silicon Laboratories
- Vice-Chair: Jérôme Quévremont, Thales Research & Technology
- develop feature and functionality roadmap and the open-source IP for the cores within the OpenHW Group such as the CORE-V Family of open-source RISC-V processors.
- Initial contribution of open-source RISC-V cores from ETH Zurich PULP Platform and the OpenHW Group is the official committer for these repositories

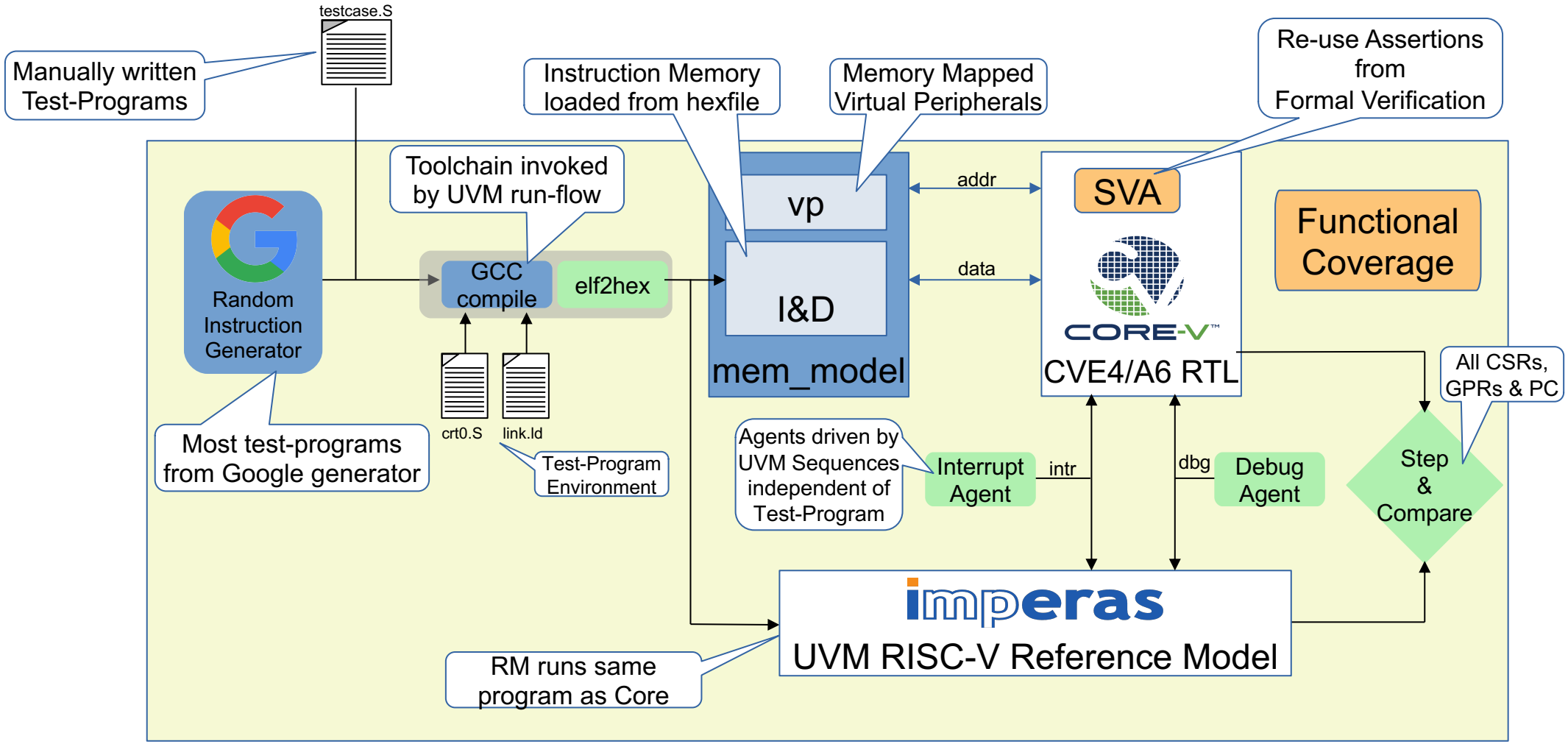
Core	Bits/Stages	Description
CVE4 (RI5CY)	32bit / 4-stage	A family of 4-stage cores that implement, RV32IMFCXpulp, optional 32-bit FPU, instruction set extensions for DSP operations including HW loops, SIMD extensions, bit manipulation and post-increment instructions.
CVA6 (Ariane)	32 & 64bit / 6-stage	A family of 6-stage, single issue, in-order CPU cores implementing RV64GC extensions with three privilege levels M, S, U to fully support a Unix-like (Linux, BSD, etc.) operating system. The cores have configurable size, separate TLBs, a hardware PTW and branch-prediction (branch target buffer, branch history table and a return address stack).

Verification Task Group

- Co-Chairs:
  - Robert Chu, Futurewei Technologies, Inc.
  - Steve Richmond, Silicon Laboratories

- develop best in class verification test bench environments for the cores and IP blocks developed within the OpenHW Group.

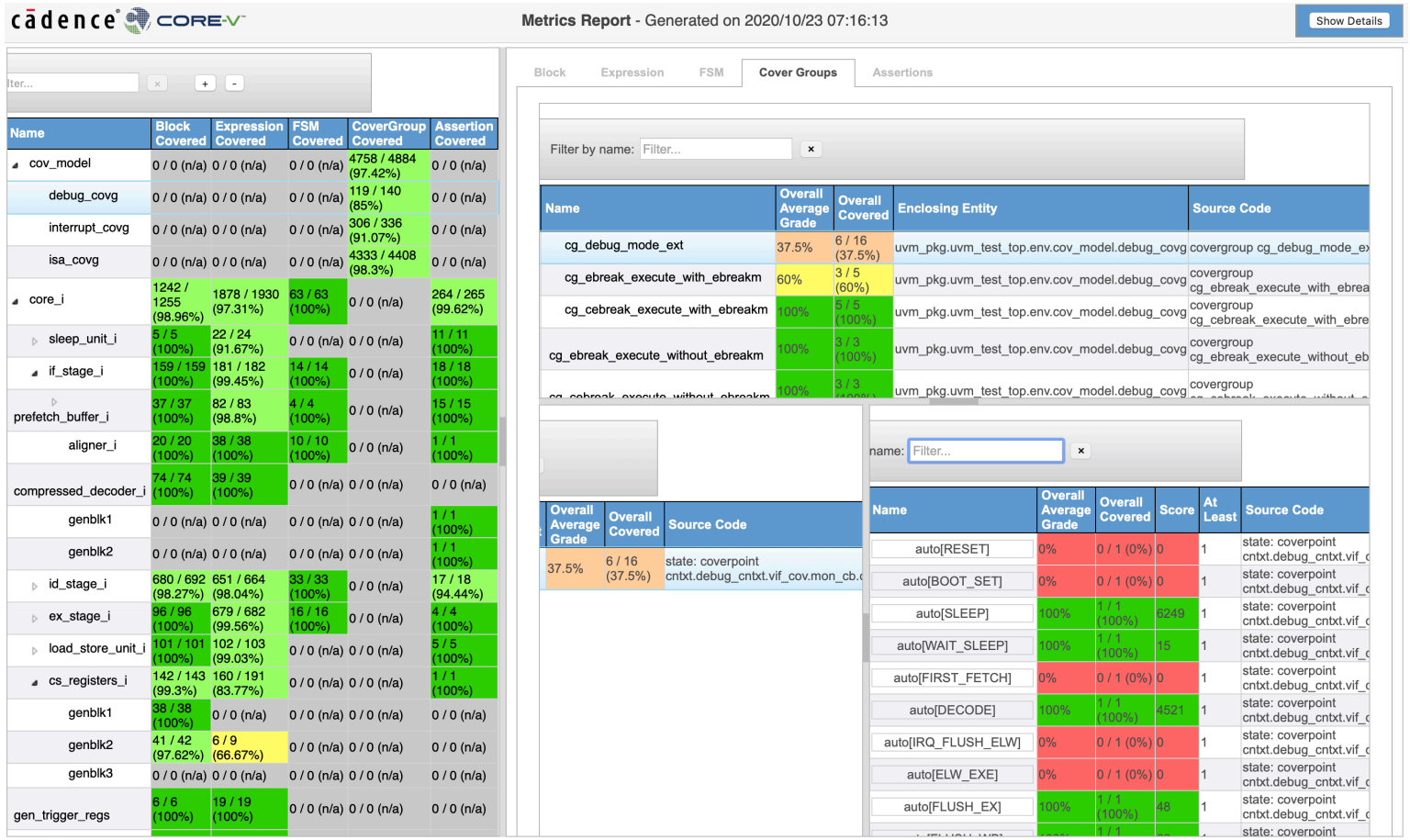
CORE-V Verification UVM Test Bench



make SIMULATOR=<sim> +UVM_TEST=riscv-dv-test

CV32E4 'RTL Freeze' Coverage Data

- CV32E4 Coverage Data published in our core-v-verif github repo
- Coverage told us we had…
  - Bugs in the functional coverage model
  - Low coverage in Instructions Exceptions testing
  - Low coverage of Int & Dbg corner-cases
  - Low coverage of Instruction and Data bus interface protocol



SW Task Group

- Chair: Jeremy Bennett, Embecosm
- Vice-Chair: Yunhai Shang, Alibaba T-Head

- define, develop and support SW tool chain, operating system ports and firmware for the cores and IP developed within the OpenHW Group.

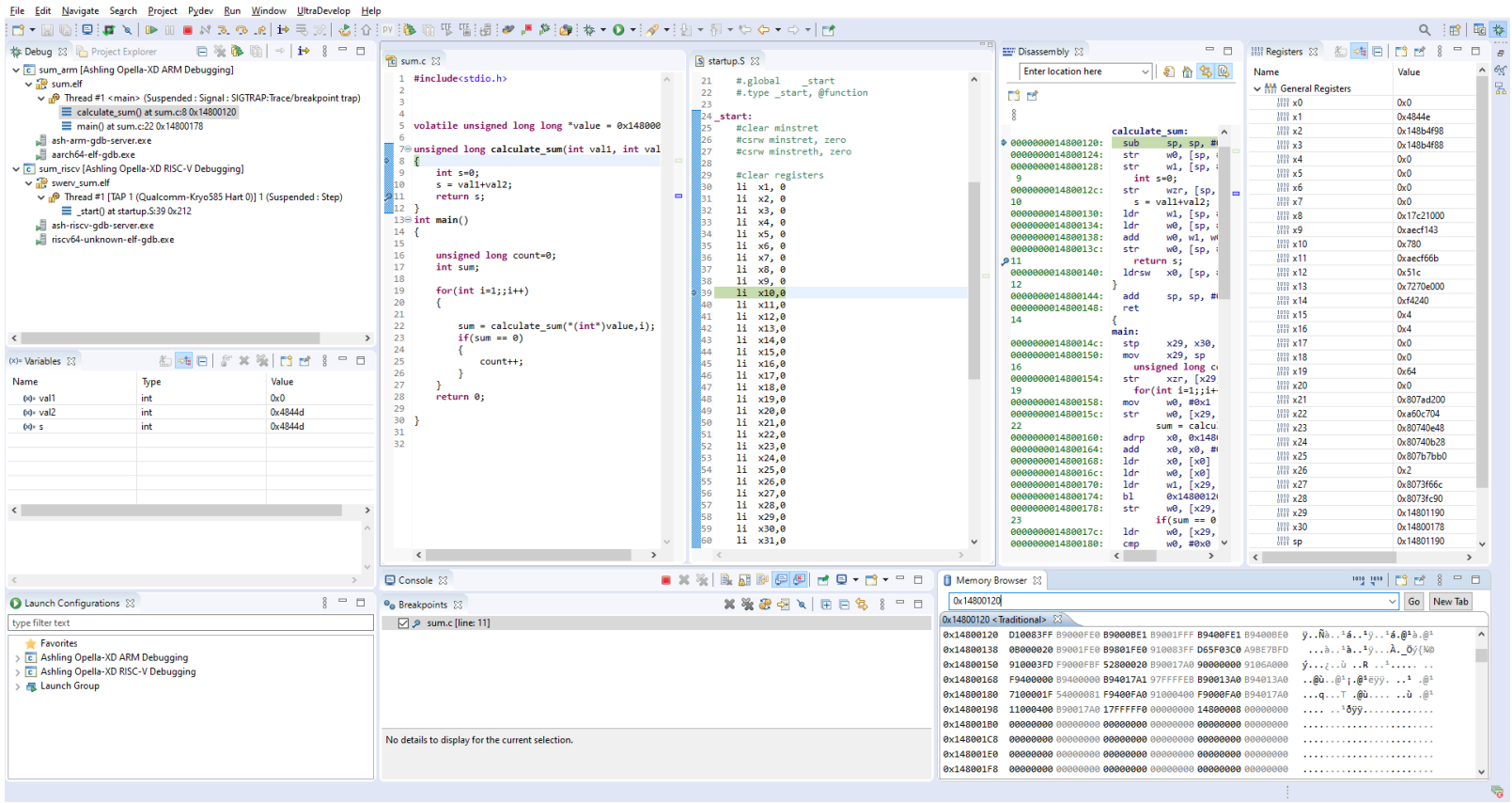
CORE-V™ IDE

ASHLING

EMBECOSM®

CORE-V™

- CORE-V IDE is an open-source development under the SW TG at the OpenHW Group
- Eclipse based IDE for CORE-V development
- Includes the GCC Toolchain for CORE-V
- OpenOCD Debug Support
- “Ready-to-run” examples for Digilent FPGA boards
- Getting started guides



IAR SYSTEMS

PlatformIO labs

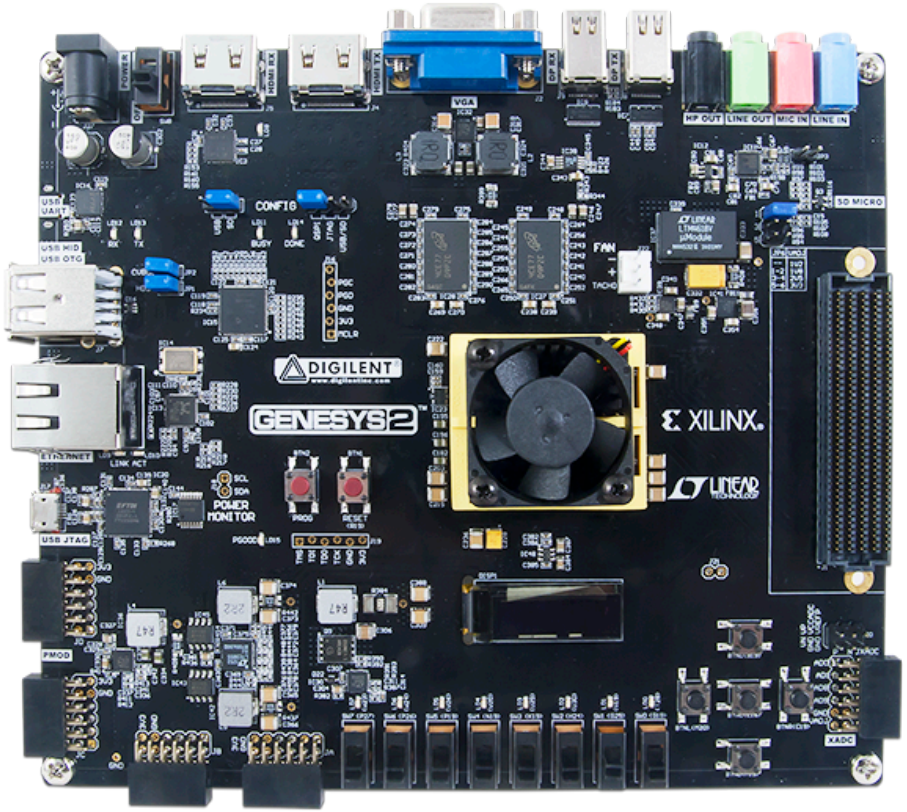
HW Task Group

- Chair: Hugh Pollitt-Smith, CMC Microsystems
- Vice-Chair: Tim Saxe, QuickLogic
- define, develop and support SoC and FPGA based evaluation / development platforms for the cores and IP developed within the OpenHW Group.

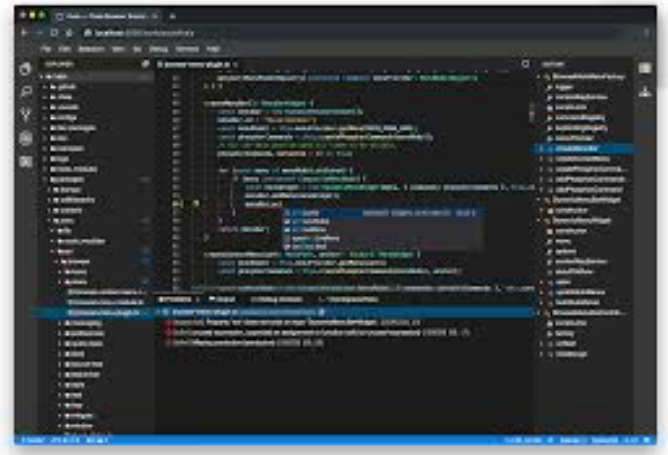
CORE-V™ FPGA Development

- Initial project using Digilent Genesys2 FPGA boards for soft-core bring up for both CV32E4 and CV64A6

Digilent Genesys2



JTAG Probe



IDE

CORE-V™ MCU SoC Tapeout 1st half 2021

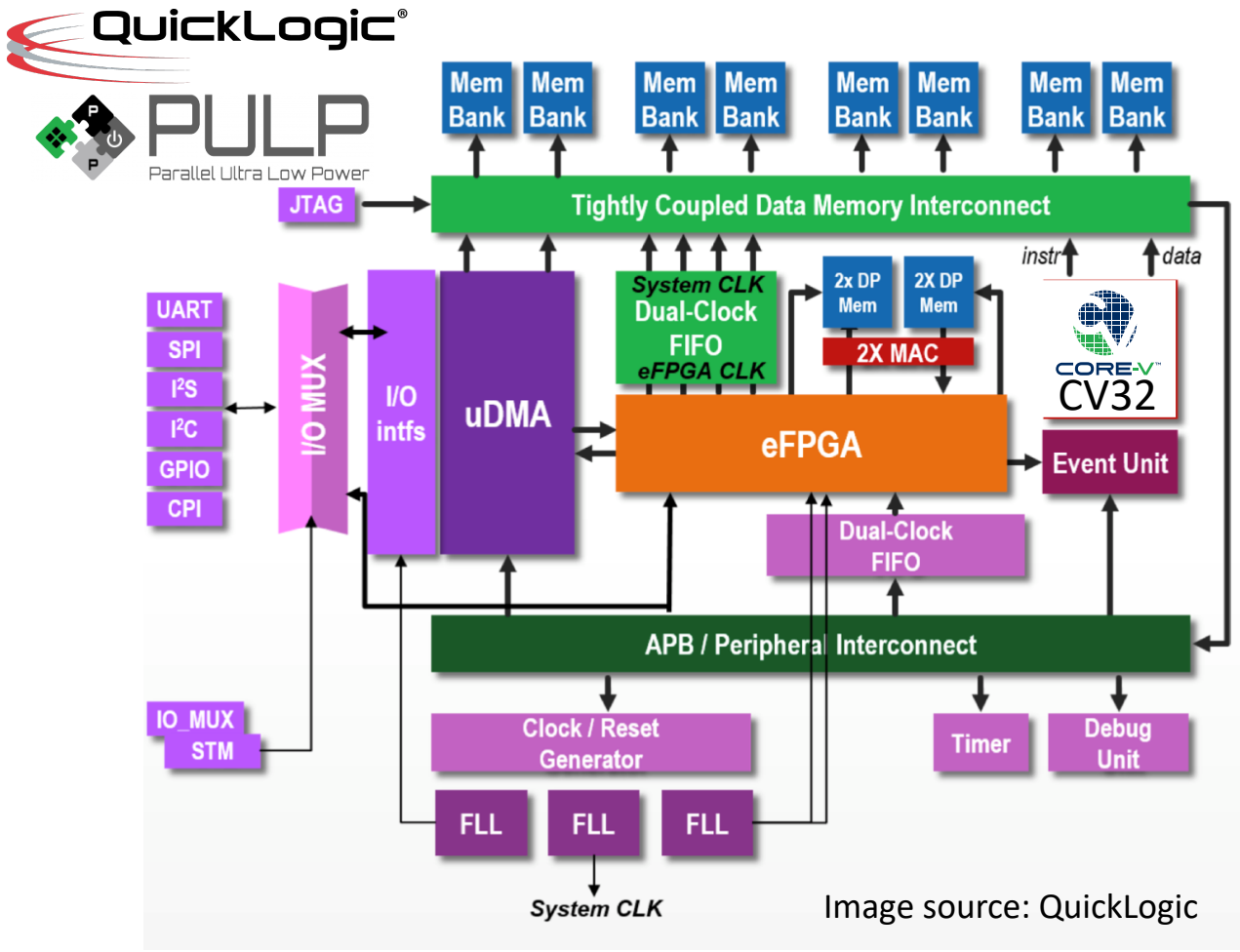


Image source: QuickLogic

- Real Time Operating System (e.g. FreeRTOS) capable ~600+MHz CV32E4 MCU
- Embedded FPGA fabric with hardware accelerators from QuickLogic
- Multiple low power peripheral interfaces (SPI, GPIO, I2C, HyperRAM, CAMIF, etc) for interfacing with sensors, displays, and connectivity modules
- Built in 22FDX with GF

OpenHW Accelerate

- Multi Year research initiative totaling up to $22.5M USD of co-funded research
  - Up to $4.5M USD research funding per year
  - Funding available globally across Canadian and International Universities (75% Canadian / 25% International)
  - Available to Silver and above OpenHW Group member organizations
- OpenHW Accelerate managed within OpenHW Marketing Working Group, University Outreach Task Group Co-Chaired by Mitacs and CMC
  - Establishes project approval process
  - Peer Review Committee drawing on Academic and Industry subject matter experts for project approvals

OpenHW Accelerate 1st Project

- 1st OpenHW Accelerate Co-Funded Project

  CORE-V CV-VEC: RISC-V Vector Processor for High-throughput Multidimensional Sensor Data Processing & Machine Learning Acceleration at the Edge

  - Gord Harling, CEO, CMC (Industry Sponsor)
  - Frank Gürkaynak, Director, Microelectronics Design Center, ETH Zürich
  - Matheus Cavalcante, PhD Candidate, ETH Zürich
  - Yvon Savaria, Professor, Electrical Engineering, Polytechnique Montréal
  - Hossein Askari Hemmat, PhD Candidate, Polytechnique Montréal

What's Next? Some Predictions...

1. OpenHW Group ecosystem continues to grow
   - Over 80 Members & Partners expected by end of 2021

2. New open-source RISC-V cores added to the CORE-V Family
   - CV32E4 and CV64A6 now – CV32E2, CV32A6, CV32E4 variants and more to come

3. On chip SoC interconnect (fabric & busses)

4. Heterogeneous clusters with accelerators and leveraging eFPGA

- OpenHW Group & CORE-V Family of open-source RISC-V cores
  - Visit www.openhwgroup.org for details
  - Learn more at OpenHW TV
- Follow us on Twitter @openhwgroup & LinkedIn OpenHW Group

Day 1st April 2021

Time	Speaker, Chair	Title
08h30	Rick O'Connor	Keynote – Open Source History, Trends & Adoption
09h30	Davide Schiavone, Jérôme Quévremont	CORE-V Cores Roadmap
10h30	Robert Balas, Jeremy Bennett, Simon Davidmann, Alexander Fedorov, Alfredo Herrera, Ivan Kravets, Philipp Krones, Jessica Mills, Shteryana Shopova	OpenHW SW Task Group Projects
12h00		Lunch
12h30	Rick O'Connor. Luca Benini, Fabien Clermidy, Simon Davidmann, John D. Davis, Mike Milinkovich, Matthias Völker, Tim Whitfield.	Panel – OpenHW Europe
13h30	Florian Zaruba	CORE-V MCU & APU
14h30		Break
14h45	Aimee Sutton, Lee Moore, Mike Thompson, Steve Richmond, Greg Tumbush	CORE-V Verif: Hands On
16h15	Rick O'Connor. Sebastian Ahmed, John Martin, Robert Oshana, Tim Saxe, Jérôme Quévremont	Panel – OpenHW IP Adopters
17h15	Duncan Bees	OpenHW Project Execution
17h45	Rick O'Connor	OpenHW Day Wrap Up
18h00		End of OpenHW Day