Deterministic Cache Coherent ManyCore Environment for Embedded Systems

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***Abstract*—Embedded Systems has brought a revolution to the world. It is part of the Internet of Things which involves everyone even objects and animals. Embedded systems perform specific tasks thus they can be optimized to reduce the size and cost of the system and increase the reliability and performance. Most of the time, embedded systems require determinism and it is critical to the operation of the overall system. Unfortunately, there is no open source platform for Embedded Systems research. In our work we propose a deterministic cache coherent many-core environment for Embedded systems based on cva6[1] and OpenPiton[2]**

I. Motivation and methodology

Rumors about the death of Moore's law are everywhere. The observation made by Gordon Moore in 1965 that the number of transistors, hence the computing power, in a dense integrated circuit doubles about every two years. Based on these rumors, there has been a huge movement in research and industry to move away from the clung of building one complex sophisticated core with very high frequency to having many cores two, four, eight, .. or even a million of simple, low power, and low frequency to achieve exponential growth in power saving and performance. We tried to make an automated flow that transforms your one core RISC-V system on chip to cache coherent many core system using OpenPiton and then we are proposing some ideas on how to make it much more suitable to target Embedded Systems.

OpenPiton is a powerful platform for instruction set architecture and systems research. OpenPiton provides a configurable and scalable cache coherence system that -for now- supports four main instruction sets RISC-V 32, RISC-V 64, SPARC v9, x86. It is connected to more than seventy cores and it supports running SMP linux. OpenPiton is totally open source and written in industry standard hardware description languages Verilog and SystemVerilog.

Nowadays there are multiple platforms such as OpenPiton that are used for ISA and systems research but mostly for high performance systems that require solid cache coherency protocal and distributed L2 cache, but there isn't any platform intended for Embedded Systems Computing. Our goal is to use OpenPiton to generate a baseline cache coherent small cva6 cluster two or four core and then update the cache systems to match Embedded Systems deterministic latency requirements

II. Current development

Up till now OpenPiton has been used to compare between different cores and ISAs inside its own environment. However, We used OpenPiton to generate a network many core cache coherent system. We took the cache coherent domain part of the system -as shown in the figure- outside of OpenPiton, and neglect other peripherals bootroom, memory controller, UART, PLL, .. etc, then we used a NoC to AXI transducer, and finally connected the chip with AXI interface to our SoC. The flow is generic and can be used by anyone in a systemaic way to build his own cache coherent many core network using any of fiften cores already connected to OpenPiton and tested.

We also extended the OpenPiton environment with micro-benchmarks[3] to measure the performance of the generated cache coherence domain in terms of pipelined memory access latency, back to back access latency, restart latency, and also measuring the headache coming from the coherency protocol.

Our goal is to make a small cluster of two or four cores with cva6 with a cache sytem optimized for Embedded systems. We already used the proposed flow with OpenPiton to generate a base line for our project, a dual core ariane. Next, we are going to work on the cache enhancements.

III. Conclusion and future work

To conclude, there are no available open source platforms for Embedded Systems as for example the case with OpenPiton having solid cache coherency protocol and distributed l2 cache you can't have by any means a good deterministic latency with good performance. As the deterministic latency will be longest path latency plus longest coherency latency. We will focus on the possibility of using OpenPiton to generate a baseline and update it for Embedded Systems achieving the best determinism and performance.

References

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