ControlPULP: A Multi-Core RISC-V Power Controller for HPC Processors

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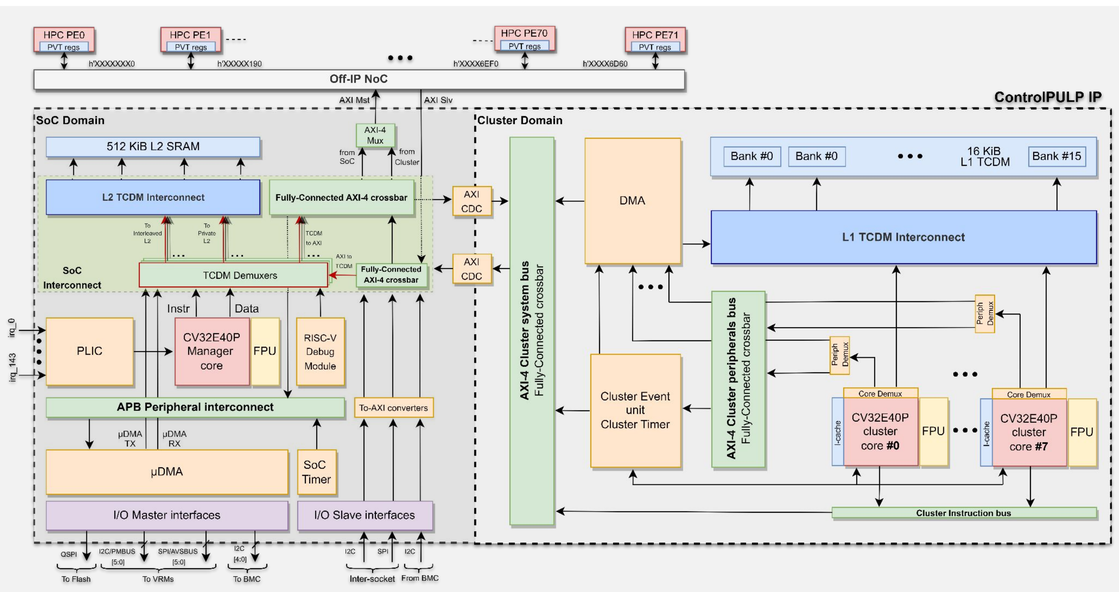
1 Why an integrated multi-core Power Controller?

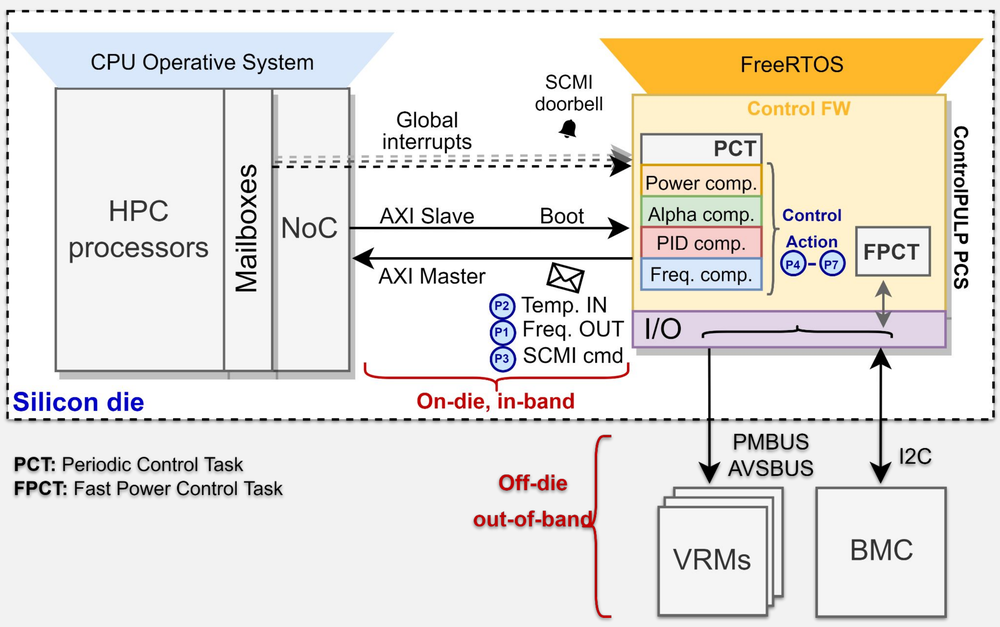
- Integrated **Power Controller Systems (PCS)** are key elements for governing the power consumption of modern HPC servers[1].
- RISC-V lacks a reference design to conduct on-chip power management.
- More **scalable and flexible** PCS architectures are required to support advanced MIMO control algorithms and track PVT variability than single-core SoA solutions[2].

2 The ControlPULP platform



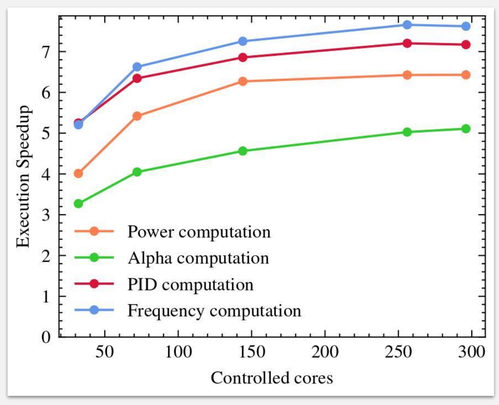
- **Scalable architecture:** multi-core cluster with private FPUs, DMA for PVT sensor data acquisition, low-latency PLIC interrupt controller.
- **Power management interface:** AVSBUS/PMBUS for off-chip VRMs interaction, ARM SCMI for on-chip OS interaction.

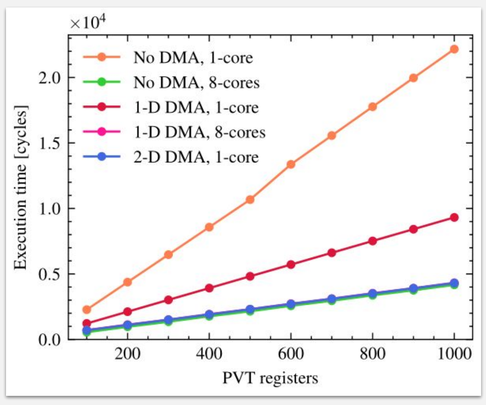
3 The Power Control Firmware

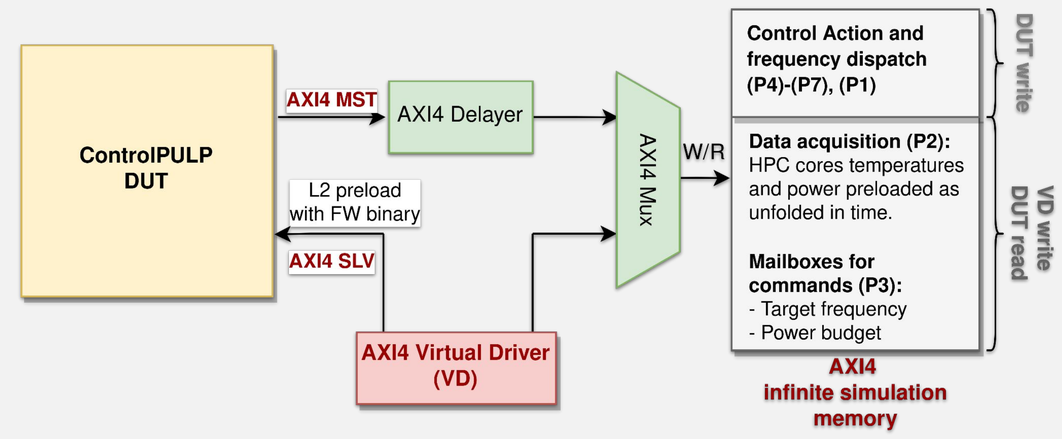


- **Per-core** power regulation.
- Relies on industry-grade Real-Time OS, **FreeRTOS**.
- **Periodic Control Task** (PCT, 2 kHz) and **Fast Power Control Task** (FPCT, 8 kHz) tackle OS and BMC operating point and power budget requests respectively.
- Compares favorably with SoA and open standard FW, IBM OCC (6% more precise setpoint tracking on heavy workloads).

4 Evaluation







- RTL Cycle-accurate simulation framework.
- PCF acceleration leads to overall **4.9x speedup** with multi-core cluster execution and 2-D DMA-based PVT registers data acquisition against single-core, non-DMA based execution.

5 Conclusion

- The **first fully open-source** (HW/SW) RISC-V parallel PCS with configurable number of cores and interfaces.
- Designed to track the computational requirements of **current and future HPC processors**.

[1] G. Bambini *et al.*, "An Open-Source Scalable Thermal and Power Controller for HPC Processors," 2020.
[2] R. Schöne, T. Ilsche, M. Bielert, A. Gocht and D. Hackenberg, "Energy Efficiency Features of the Intel Skylake-SP Processor and Their Impact on Performance," 2019.

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