Variability-aware Deep Sub-micron Low-energy Designs for IoT RISC-V Processors

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With the ever-increasing demand for smart devices and battery-operated IoT gadgets, the design of low-energy micro-controllers becomes a high-value market. Since most IoT devices are battery-operated, these micro-controllers become energy constrained. To achieve low energy consumption, research shows that aggressive voltage scaling to near-threshold regime results in minimum energy point operation [1]. With the scaling of technology nodes to deep sub-micron structures, a trend to lower threshold voltages is observed. Combined with the need for ever more complex designs, the use of deep sub-micron technology nodes is justified. However, aggressive voltage scaling to near-threshold operation in these nodes comes at a risk: transistor variation increases. Hence, the standard design paradigm of using margins leads to large overheads, nulling the energy savings of lower technology nodes. This work provides an overview of detection methods to reduce design margins, allowing circuits to run close to the Point of First Failure. Variation of digital designs can be split up into two sections: (1) a logic section, expressed as timing margins and (2) a memory section, expressed as Static Noise margin. Timing margins in logic designs can be reduced by the introduction of double sampled flipflops [2] or transition detectors [3]. Retention of memory cells can be monitored using replica monitors [4]. However, both logic and memory designs require an additional error processor and a feedback mechanism to be able to operate with these close margins at run-time. This work shows how the RISC-V architecture, with its open source strategy, allows for an easy design to make these micro-controllers variation-aware, providing an opportunity to safely remove the unnecessary margins inserted during traditional design flows at run-time, thus increasing the energy-efficiency.

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[2] H. Reyserhove and W. Dehaene, “A Differential Transmission Gate Design Flow for Minimum Energy Sub-10-pJ/Cycle ARM Cortex-M0 MCUs,” *IEEE Journal of Solid-State Circuits*, vol. 52, no. 7, 2017, doi: 10.1109/JSSC.2017.2693241.

[3] R. Uytterhoeven and W. Dehaene, “Completion Detection-Based Timing Error Detection and Correction in a Near-Threshold RISC-V Microprocessor in FDSOI 28 nm,” *IEEE Solid-State Circuits Letters*, vol. 3, pp. 230–233, 2020.

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