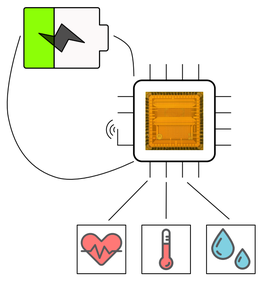
# Variability-aware Deep Sub-Micron Low-Energy Designs for IoT RISC-V Processors

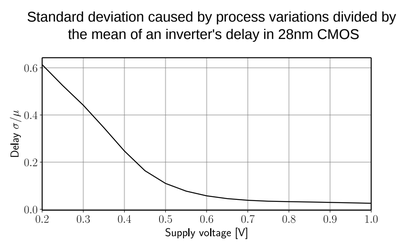
**Bob Vanhoof, Clara Nieto Taladriz, Wim Dehaene**

MICAS, Department of Electrical Engineering (ESAT), KU Leuven

## IoT minimum energy consequences

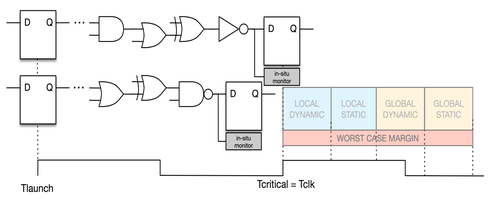


Energy efficiency
↓
Near-threshold operation
↓
Higher impact of variability
↓
Larger design margins
↓
Decrease Energy efficiency!!



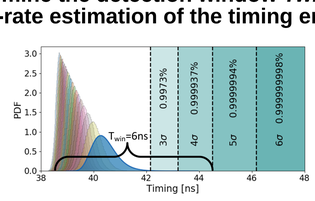

## Timing variability

**Solution: Remove margins by detecting the Point of First Failure (PoFF) via in-situ time monitoring**

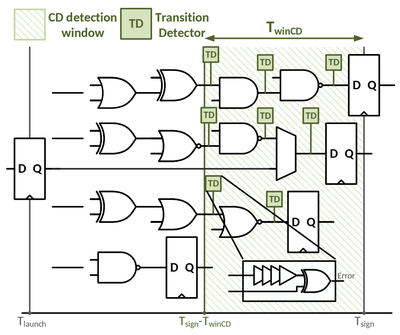



### Strategy: RISC-V with Completion Detection (CD)

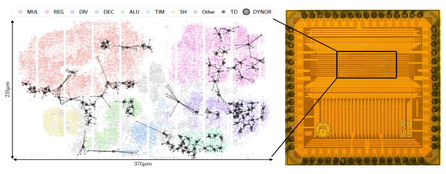
1. Determine the detection window *Twin*: via the error-rate estimation of the timing error PDFs.



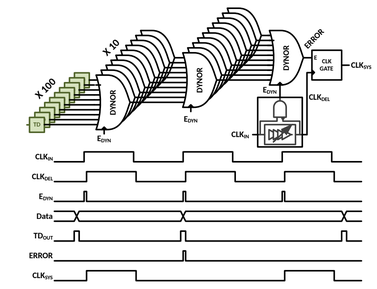

2. Identify the critical cells according to *Twin* and place a transition detector (TD) next to them.




3. OR the TDs output. Find semi-optimal placement for DYN-OR gates based on the TDs physical location.




TDs and DY-OR elements in the core area of RISC-V processor




4. Error correction integration. This work: clock gating/stretching.

### Strategy: RISC-V with Endpoint detection (ED)




1. Choose: error detection or error prediction.




2. Determine the number of monitors to insert and their detection window (DW) size.
3. OR TDs output based on the physical location.
4. Error correction? If prediction no needed.

### Strategy: Block-oriented Endpoint detection

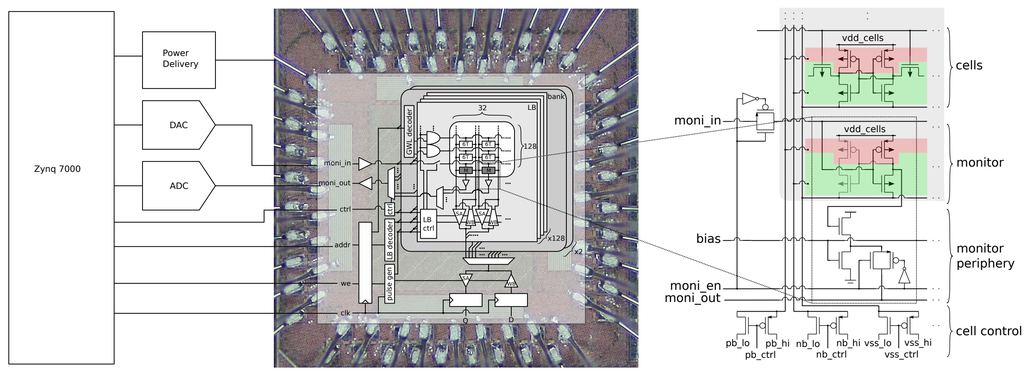
**Target: Register File, as its power consumption is 47.5% of the RISC-V total consumption.**



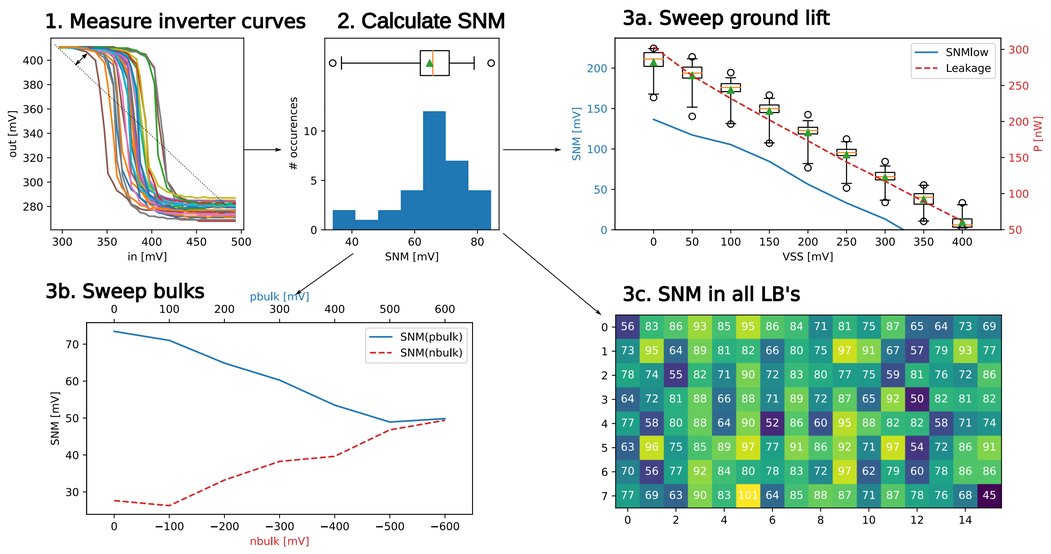

## Static Noise Margin in memory cells

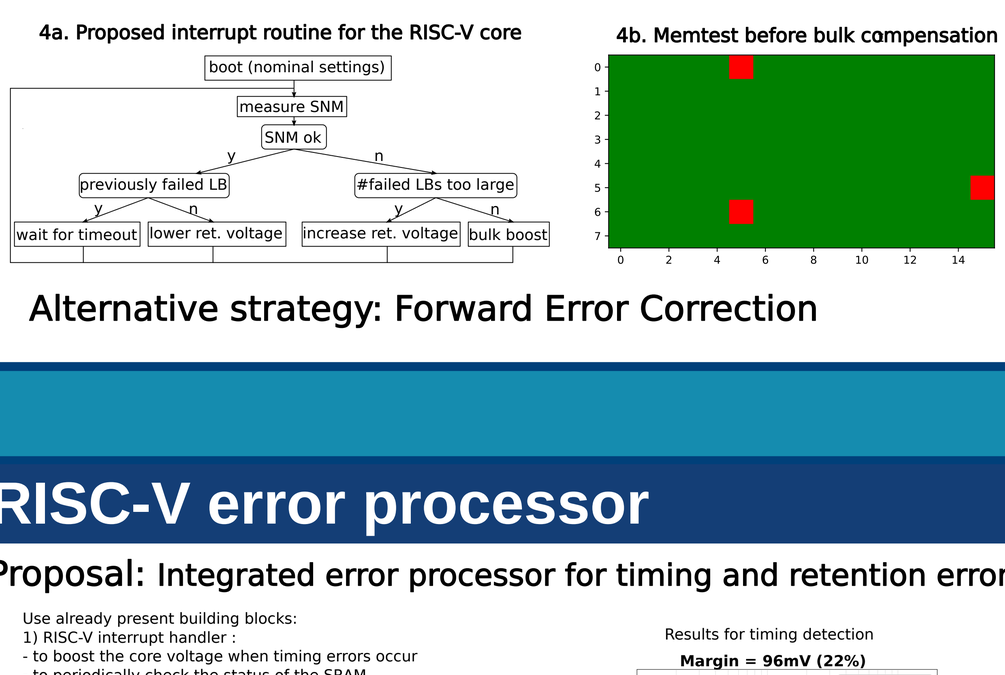
Strategy: Replica monitors in each local block for individual block compensation, controlled by RISC-V

**SYSTEM OVERVIEW**




**SNM MEASUREMENT**



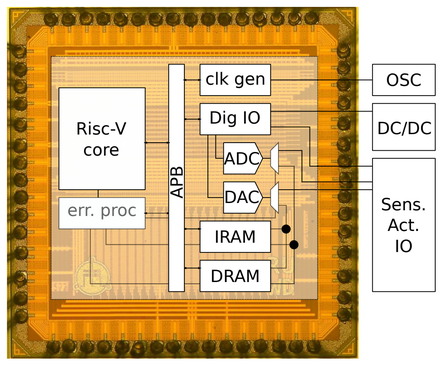




Alternative strategy: Forward Error Correction

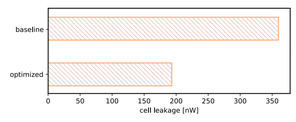
## RISC-V error processor

Proposal: Integrated error processor for timing and retention errors

Use already present building blocks:
1) RISC-V interrupt handler :
- to boost the core voltage when timing errors occur
- to periodically check the status of the SRAM
2) ADC/DAC pair: test of the SRAM monitors

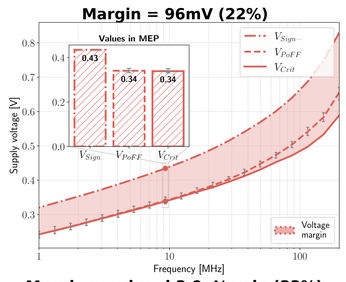



Results for SRAM retention with bulk compensation

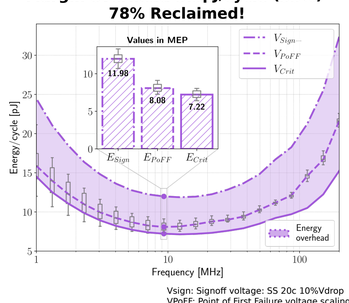



Results for timing detection

**Margin = 96mV (22%)**




**Margin overhead 3.9pJ/cycle (33%)**
**78% Reclaimed!**




Vsign: Signoff voltage: SS 20c 10%Vdrop
VPoFF: Point of First Failure voltage scaling
Vcrit: Critical voltage where processor fails.

[1] W. Dehaene, R. Uyterhoeven, C. Nieto Taladriz Moreno, and B. Vanhoof, “Dealing with the Energy Versus Performance Tradeoff in Future CMOS Digital Circuit Design,” 2020. doi: 10.1007/978-3-030-18338-7_7.
[2] H. Reyserhove and W. Dehaene, “A Differential Transmission Gate Design Flow for Minimum Energy Sub-10-pJ/Cycle ARM Cortex-M0 MCUs,” IEEE Journal of Solid-State Circuits, vol. 52, no. 7, 2017, doi: 10.1109/JSSC.2017.2693241.
[3] R. Uyterhoeven and W. Dehaene, “Completion Detection-Based Timing Error Detection and Correction in a Near-Threshold RISC-V Microprocessor in FDSOI 28nm,” IEEE Solid-State Circuits Letters, vol. 3, pp. 230–233, 2020.
[4] B. Vanhoof and W. Dehaene, “SRAM With Stability Monitoring and Body Bias Tuning for Biomedical Applications,” IEEE Solid-State Circuits Letters, vol. 5, pp. 29–32, 2022, doi: 10.1109/LSSC.2022.3151216.