RVfpga: Understanding Computer Architecture

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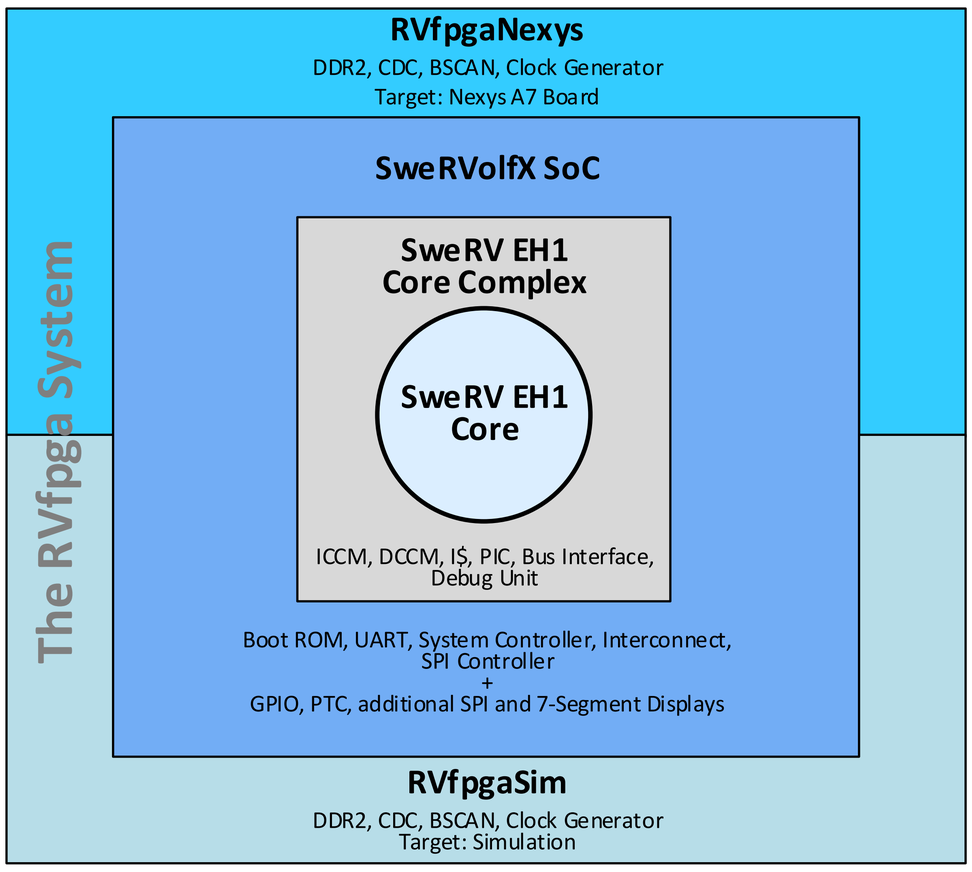
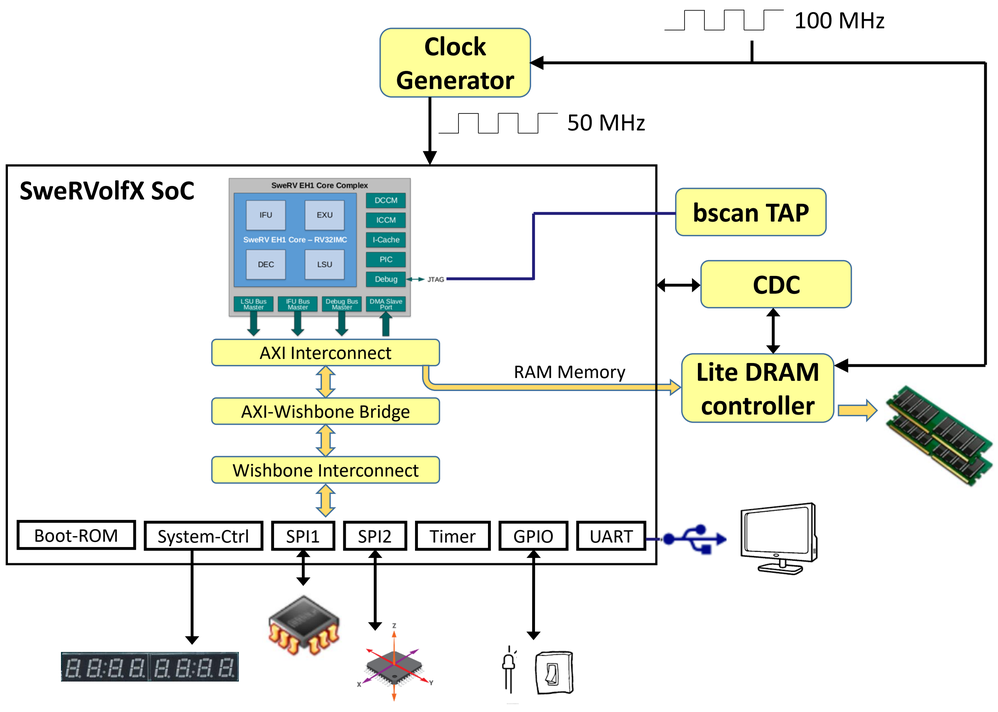
Introduction - The RVfpga Project

- RISC-V FPGA (RVfpga) is a teaching package that provides a **comprehensive**, **freely distributed**, and **complete RISC-V course** that allows students to **learn about the RISC-V ecosystem**.
- The package includes **two courses**:
  - **RVfpga**: Includes a GSG and 20 labs that show how to:
    - Target RISC-V SoC to Nexys A7 FPGA and to Simulator
    - Program the RISC-V SoC
    - Use and modify the I/O system of the SoC
    - Analyse and modify RISC-V core and memory hierarchy
  - **RVfpga-SoC**: Includes 5 labs which show how to:
    - Build a RISC-V SoC using Vivado Block Design
    - Build a RISC-V SoC using FuseSoC
    - Install Zephyr RTOS
    - Run several programs, including a Tensorflow program
- **Target audience**: Academics, industry professionals, researchers, students and everyone interested in RISC-V.
- **Expected Prior Knowledge**: Digital design; High-level and Assembly programming; Microarchitecture; Memory systems.
  Covered in "Digital Design and Computer Architecture: RISC-V Edition", Harris and Harris, Morgan Kaufmann 2021.

The RVfpga System



RVfpgaNexys:



Software and Hardware

SOFTWARE
Xilinx **Vivado** 2019.2 WebPACK
PlatformIO – an extension of Microsoft's **Visual Studio Code –** with Chips Alliance platform, which includes: RISC-V Toolchain, OpenOCD, Verilator HDL Simulator, WD Whisper instruction set simulator (ISS)

HARDWARE*
Digilent's **Nexys A7** / Nexys 4 DDR FPGA Board

*Optional: All labs can be completed in simulation only.

RISC-V CORE & SOC
Core: Western Digital's **SweRV EH1****
SoC: Chips Alliance's **SweRVolf****

**Open-source – and provided as part of RVfpga package.

RVfpga Labs

	#	Title
Part 1	0	RVfpga Labs Overview
	1	Creating a Vivado Project
	2	C Programming
	3	RISC-V Assembly Language
	4	Function Calls
	5	Image Processing: Projects with C & Assembly
	6	Introduction to I/O
	7	7-Segment Displays
	8	Timers
	9	Interrupt-Driven I/O
	10	Serial Buses
Part 2	11	SweRV EH1 Configuration and Organization. Performance Monitoring
	12	Arithmetic/Logical Instructions: the add instruction
	13	Memory Instructions: the lw and sw instructions
	14	Structural Hazards
	15	Data Hazards
	16	Control Hazards. Branch Instructions: the beq Instruction. The Branch.
	17	Superscalar Execution
	18	Adding New Features (Instructions, Hardware Counters) to the Core
	19	Memory Hierarchy. The Instruction Cache.
	20	ICCM and DCCM (Instruction and Data Closely-Coupled Memories)

RVfpga-SoC Labs

#	Title
1	Introduction to RVfpga-SoC
2	Running Software on the RVfpga SoC
3	Introduction to SweRVolf and FuseSoC
4	Building and Running Zephyr on the RVfpga SoC
5	Running Tensorflow Lite on SweRVolf

Ongoing Developments - 2022

- RVfpga **EdX Course**
- RVfpga extended to **SweRV EL2**
- **Other boards**: Basys 3, Arty A7, Virtual Development Board.
- Support for **Catapult SDK**
- 1-day **Tutorials**: US, Europe (HiPEAC June 22nd), Asia...

Academic and Industry Partners

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