The MEEP FPGA Shell

MEEP — A cluster with 96 Xilinx USSC FPGAs aiming to support a wide variety of accelerators.

The MEEP FPGA Shell provides to the end-user a novel, flexible and open platform to work with, by giving total freedom to add or remove components and functionalities at will. It currently gives support PCIe, HBM, 10Gb Ethernet, 100GbE, and Aurora FPGA links through QSFP+ out of the box. It is open source and extensible.

Supporting the RISC-V Community

The MEEP FPGA Shell have already brought up different Open-Source RISC-V based FPGA systems.

The MEEP FPGA Shell intends to become a HUB of open-source IPs, and RISC-V base designs.

FPGA CI/CD and TCL Scripted Flow

Any MEEP FPGA Shell based design will trigger a CI/CD.

The CI/CD can be customized and completed by those jobs that are specifically defined by the EA.

Every design running under the MEEP Shell environment benefits from the scripted TCL FPGA flow.

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