THE MEEP FPGA SHELL

https://github.com/MEEPproject/

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A flexible FPGA generation tool to enable RISCV in Large Scale Platforms

The MEEP FPGA Shell

MEEP → A cluster with 96 Xilinx U55C FPGAs aiming to support a wide variety of accelerator.

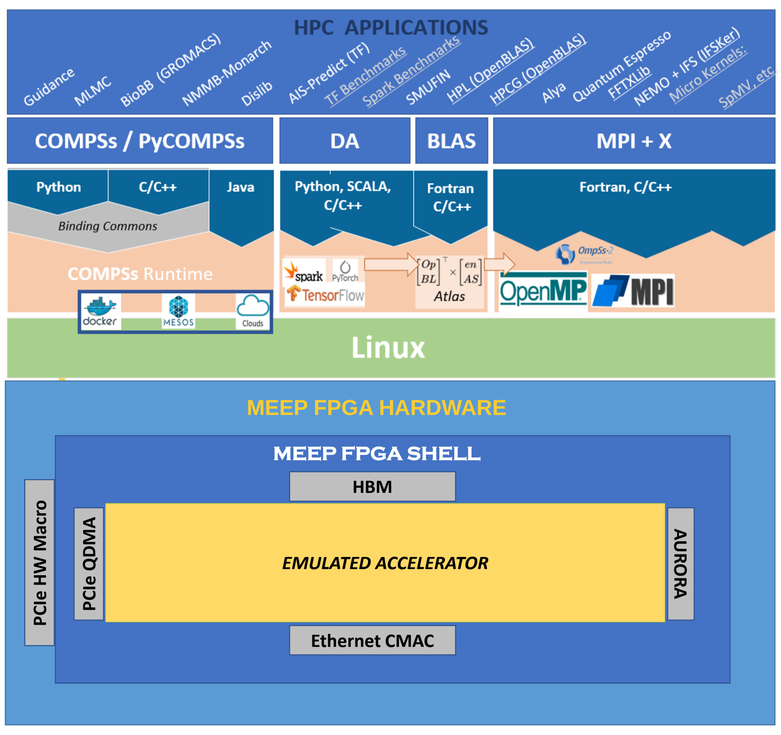
The MEEP FPGA Shell provides to the end-user a novel, flexible and open platform to work with, by giving total freedom to add or remove components and functionalities at will. It currently gives support PCIe, HBM, 10Gb Ethernet, 100GbE, and Aurora FPGA links through QSFP+ out of the box. It is open source and extensible.

MEEP is digtal laboratory for pre-silicon validation and Software Development Vehicle, compossed by up to 96 FPGAs. It is mainly focused on validating RISCV based architectures

MEEP Goals: SDV and pre-silicon validation platform

MEEP executes the whole software stack → tools and mechanisms for facing future challenges in the HPC and HPDA domains.

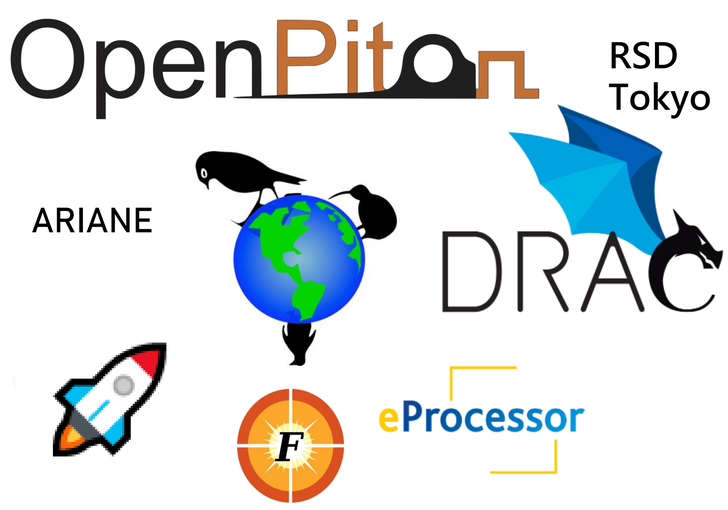
The software stack includes all the levels, from the application level to the low-level operating system services.



The whole SW and HW stack in MEEP

Supportting RISCV community

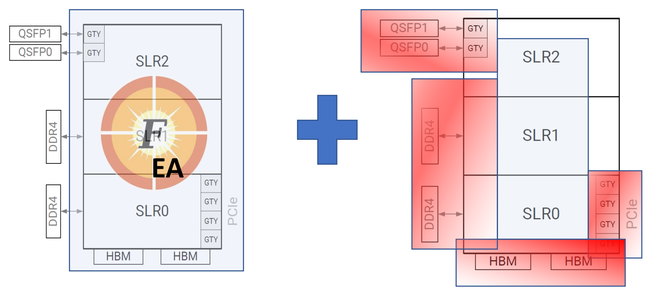
The MEEP FPGA Shell have already brought up different Open-Source RISC-V-based FPGA systems.



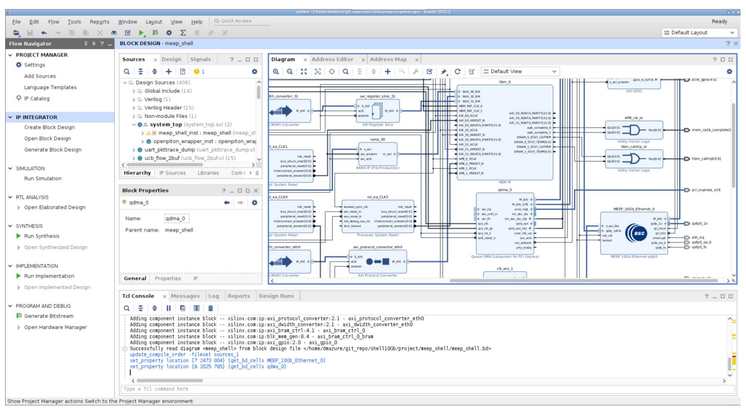
RISCV projects supported in the MEEP Shell

The MEEP FPGA Shell intends to become a HUB of open-source Ips, and RISCV base designs.

The natural evolution of the MEEP Shell Project is to become a Xilinx platform manager for RISCV processors as Vitis is now for Zynq or Microblaze.



The Emulated Accelerator (left) and the MEEP FPGA Shell (right) working together to build an Alveo RISCV Platform Out of the Box



The MEEP FPGA Shell is open, customizable to adjust to the designer needs

Shell IP	Frequency [MHz]	User Clock	Resources [LUT]
PCIe (QDMA)	250	Fixed	70376
HBM	≤ 450	Maximum	1539
Ethernet	322.26	Fixed	7444
Aurora	≤ 402.23	Maximum	1500
Aurora (DMA Mode)			4849
DDR4	300	Fixed	18823

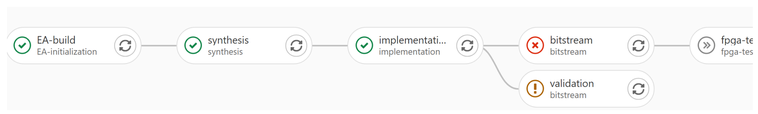
Targeted frequency and resource utilization of the different MEEP FPGA Shell components

FPGA CI/CD and TCL scripted flow

Any MEEP FPGA Shell based design will trigger a CICD.

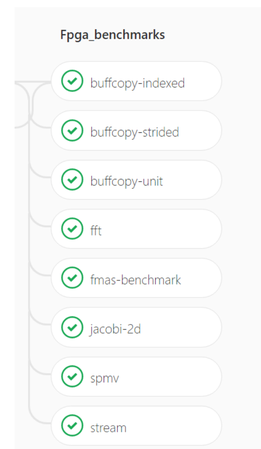
The CICD can be customized and completed by those jobs that are specifically defined by the EA.

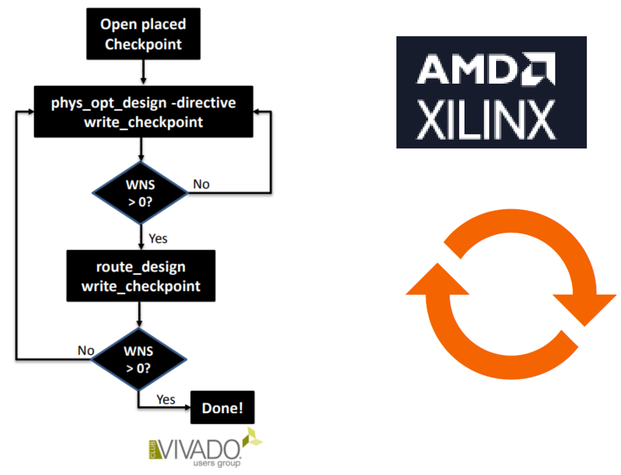
Every design running under the MEEP Shell environment benefits from the scripted TCL FPGA flow.



This CI/CD is scalable and RISC-V compatible. The MEEP FPGA Shell is constructed with placeholders for jobs that are specific to a given end-user design.

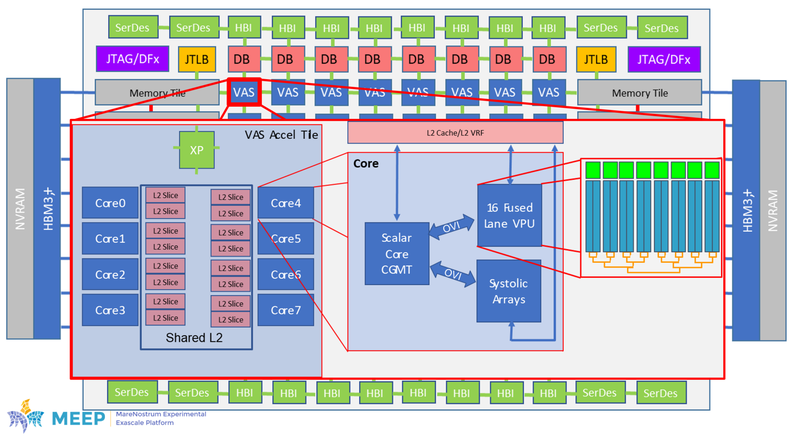
The end-user only needs to link the YAML file to the general flow to extend the MEEP FPGA Shell base functionality, as the scripted timing closure techniques. The MEEP Shell is compatible with U55C/U280 platforms and extensible to other boards.





Timing closure Vivado techniques based on TCL scripting it is a feature included on the MEEP FPGA Shell Project.

ACME as an Emulated Accelerator (EA)



Emulation platform PoC: the Accelerated Compute and Memory Engine (ACME) + the MEEP FPGA Shell.

ACME has a disaggregated architecture, and all tiles (Memory Tiles and VAS Tiles) are interconnected by a NoC.

Compute tiles: a RISC-V + a Vector Processing Unit (VPU) or/and Systolic Arrays (SA) for image processing and neural networks.

The MEEP Project has received funding from the European High-Performance Computing Joint Undertaking (JU) under grant agreement No 946002. The JU receives support from the European Union's Horizon 2020 research and innovation program and Spain, Croatia and Turkey

MEEP PARTNERS

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