Experimental Evaluation of Neutron-Induced Errors on a RISC-V Processor
Fernando Fernandes dos Santos, Angeliki Kritikakou, and Olivier Sentieys
Univ Rennes, Inria, Rennes, France

ERROR ANALYSIS
➢ RISC-V processors have been employed in smart houses, smart cities, space applications, etc. We investigated the error rate of a RISC-V processor (GAP8) exposed to a neutron beam, and classified the execution outcomes.
➢ A neutron strike may perturb a transistor’s state, generating bit-flips in memory or current spikes in logic leading to errors.

EVALUATED PLATFORM
➢ GAP8 from Greenwaves
➢ Cluster of 8+1 RISC-V cores
➢ Memory: L1 64KB, L2 512KB
➢ Core max frequency: 175MHz

PRELIMINARY RESULTS
Figure 2: GAP8’s error rate expressed as Cross Section, the number of errors observed divided by the fluence of neutrons. As cross-section depends on the number of resources used, MNIST has the highest error rate of all codes.

NEUTRON BEAM EXPERIMENTS
➢ GAP8 exposed to a neutron beam (i.e., realistic error rate)
➢ Experiments performed at ChipIR, RAL, UK
➢ Neutron flux $\approx 3.5 \times 10^6 n/cm^2/s$

Figure 3: Most incorrect executions finished with an SDC or Timed out (e.g., due to an infinite loop). SDCs are not detectable without a fault-tolerance technique. An incorrect operation due to an SDC could lead to a catastrophic event.