Agile Design Methodology for Accelerator-Rich Cluster-based RISC-V SoC

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Design trends for modern embedded heterogeneous SoCs mandate the on-chip coupling of general-purpose processors with many application-specific accelerators (e.g. ML accelerators), enabling high performance and energy efficiency.
The design and testing of these accelerator-rich systems is costly and time-consuming, motivating the need for automated hardware design flows.
High-Level Synthesis (HLS) is a widely adopted solution for designing hardware accelerators, which is mature and practical for individual IPs.
However, modelling the complex interactions of sophisticated, accelerator-rich platforms is not as easy.
Innovative approaches are essential to (i) easing the architectural exploration of accelerator-rich systems; (ii) streamlining the design, optimization, and integration of the required HW and SW components.
We propose a methodology for exploring and designing accelerator-rich heterogeneous embedded systems that leverage a template-based tool flow.
The tool relies on the extensive parametrization of a RISC-V-based platform, allowing for seamless integration of custom accelerators at the system level.
Experimental results, evaluated on heterogenous FPGA-based SoC, show how the methodology can be used to extensively characterize resource usage and performance metrics by relying on different application scenarios and exploring various architectural alternatives of the baseline platform.