# Automatic Micro-Architecture Exploration and Synthesis for RISC-V CPUs

Jean-Michel Gorius, Steven Derrien, Simon Rokicki

Univ Rennes, Inria, CNRS, IRISA
{jean-michel.gorius, steven.derrien, simon.rokicki}@irisa.fr

## Designing a RISC-V CPU should be as simple as writing an Instruction Set Simulator

### Introduction

**Context:** Increasing need for customizable architectures for embedded applications.

**Problem:** Micro-architectural design is tedious and error-prone, how do we make such customizations available to everyone?

**Our approach:** Leverage High-Level Synthesis to synthesize micro-architectures from a single instruction set simulator in C.

### Synthesizing In-Order Pipelined Instruction Set Processors

**What we have with traditional loop pipelining**

- Fully automated design toolchain
- Traditional HLS toolchain as a backend
- Based on Speculative Loop Pipelining [Derrien’2020]

**SpecHLS toolchain**

- Speculation opportunities derived from unbalanced paths in the input
- Design space exploration leveraging intertwined speculations to obtain the best designs

### Conclusion

- We need speculation to synthesize processor cores [Nurvitadhi’2011, Josipovic’2019, Derrien’2020].
- Processor design from an ISS using speculative pipelining enables fast iteration times and intuitive design exploration.

### References

