A RISC-V Heterogeneous SoC for Embedded Devices

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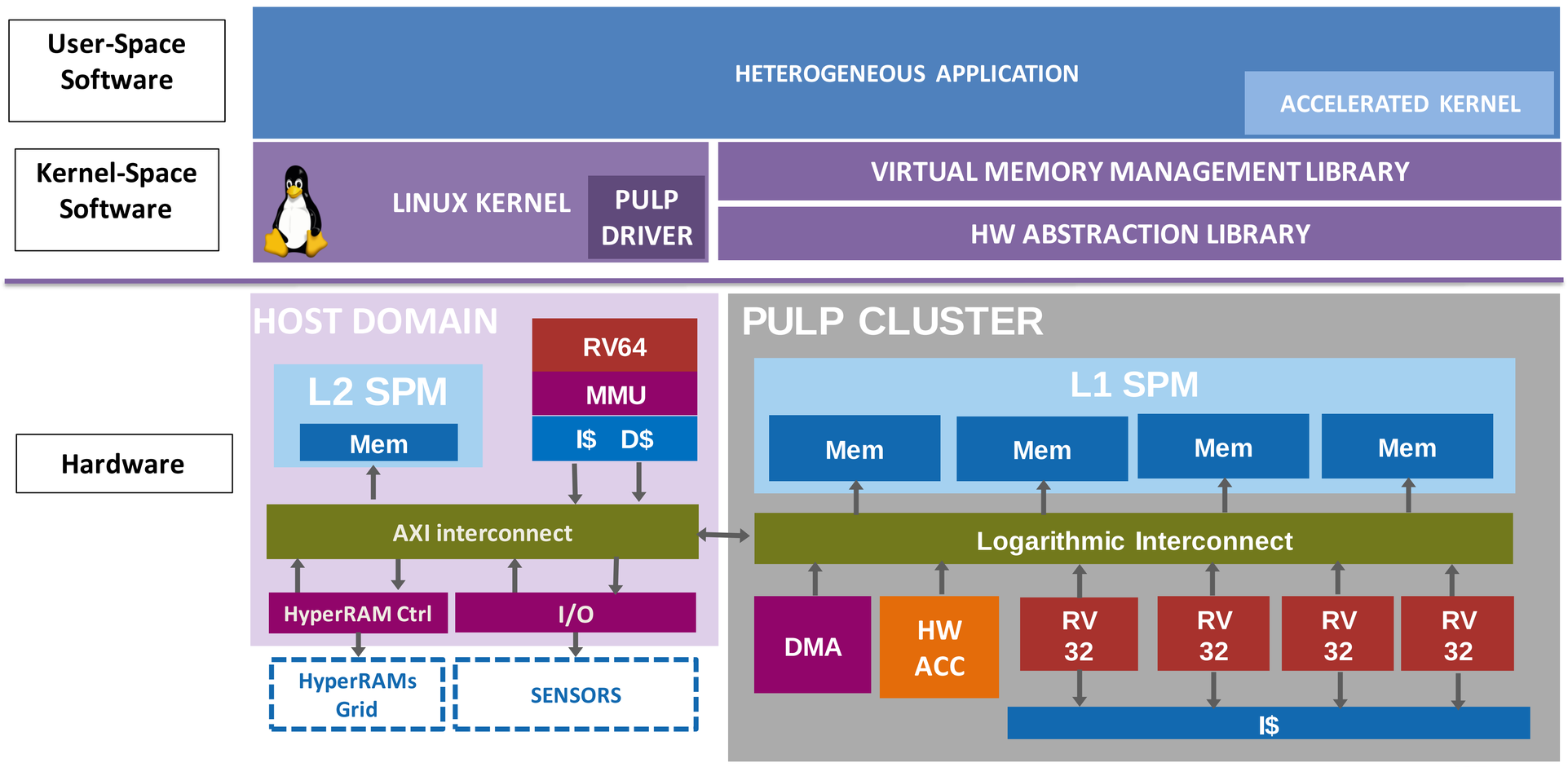
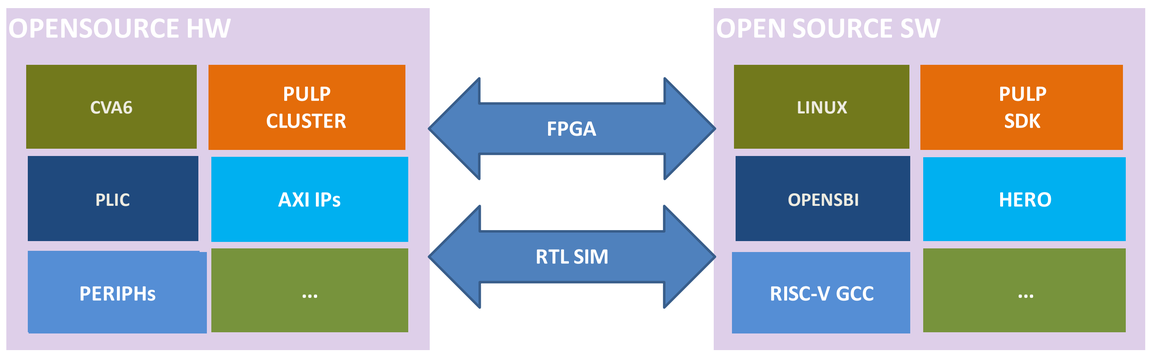
Motivations

- Heterogeneous embedded systems on chip (**HESoCs**) to combine general-purpose computing with domain-specific, efficient processing capabilities.
- **Dedicated hardware accelerators along with a general-purpose host processor**.
- **Asymmetric** multi-core architectures: small number of **"host" cores**, designed for single-thread performance, to clusters of small energy-efficient **"accelerator" cores.**
- **Fully RISC-V heterogeneous SoC for deeply embedded systems:**
  - **CVA6** [1], a 64-bit Linux-capable host CPU
  - Cluster of **8 32-bit RI5CY cores enhanced with ML and DSP extension**[2].

Hardware-Software stack



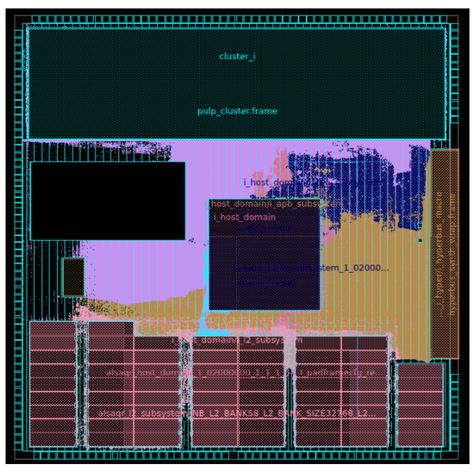
Methodologies and Milestones

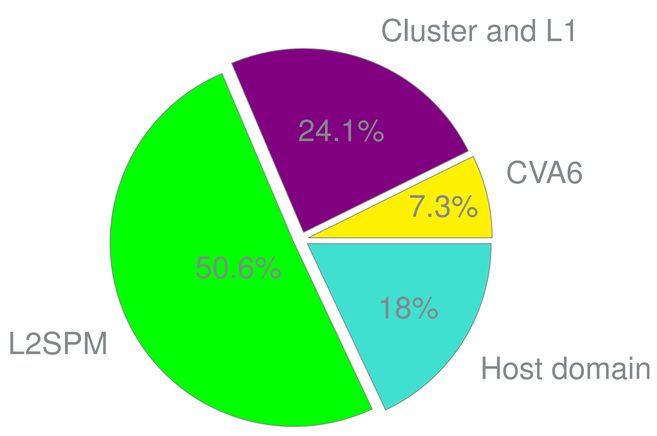


- **Almost all the IPs integrated inside the SoC are open-source**
- Allows to focus on **system integration**
- **FPGA Emulation** for faster software validation.
- **Linux boot on Xilinx VCU118**
- Machine-level tests on the cluster
- **Micro-architectural improvement for the RI5CY cores inside the cluster.**

Test-chip

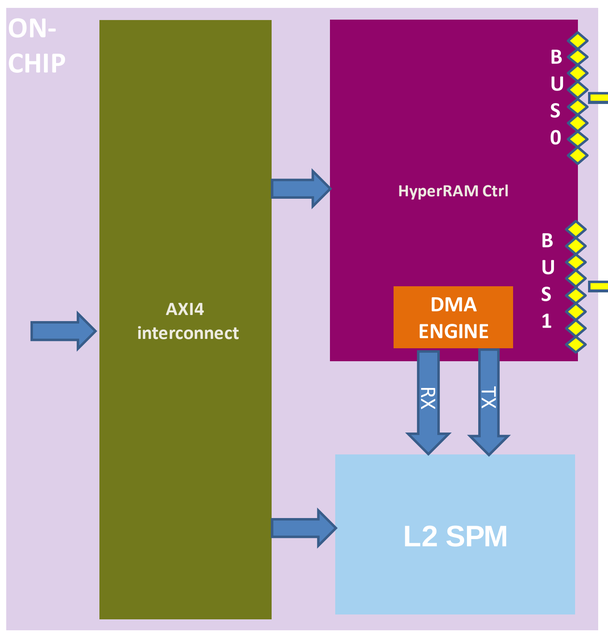
- **9mm2 tape-out in Global Foundries 22-nanometer FDSOI technology next month.**
- Below, a P&R snapshot and area breakout:





Memory Hierarchy

- Linux execution requires special attention to the memory hierarchy.
- **At least 20 MB**, unavailable on-chip.
- Usually, **mid-end embedded systems** rely on **proprietary expensive DDR/LPDDR controllers**, with **high-pin count**.
- On our side, the main memory controller is a **lightweight AXI4-to-Hyperbus** controller with **low pin-count** and embedded DMA capabilities:
  - AXI4 memory-mapped for **Linux execution (up to 64x4MB)**
  - **Interleaved** HYPERRAMs to **double bandwidth** (up to 5.312 Gbps)
  - **Contiguous** HYPERRAMs to increase capacity.
  - **Direct access to L2SPM**



Bytes Addressing	HYPERBUS 0		HYPERBUS 1	
Chip select 0	0	1	2	3
	...	...	...	...
	2N-4	2N-3	2N-2	2N-1
Chip select 1	2N	2N+1	2N+2	2N+3
	...	...	...	...
	4N-4	4N-3	4N-2	4N-1

Future development

The project aims to develop an embedded system with a focus on **real-time, reliability and security**. To this extent, these are some of the future directions of research and development:

- **Lightweight host-to-cluster offload from user space,**
- **IOPMP,**
- **IOMMU,**
- **Redundancy mechanisms.**

References

[1] "CVA6". In: (2022). URL: https://github.com/openhwgroup/cva6.

[2] "PULP cluster". In: (2022). URL: https://github.com/pulp-platform/pulp_cluster.

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