Implementing Functional Safety in a RISC-V Interleaved-Multi-Threading Processor Core

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Safety critical errors in digital microprocessors increase with the reduction of minimum feature size and voltage margins. For that reason, Functional Safety in microprocessor cores through Fault Tolerance (FT) architecture techniques, is a key requirement in several embedded application domains, especially when based on commercial-off-the-shelf (COTS) hardware components. Yet, classical Triple Modular Redundancy protection against faults occurring in any bit of the core may be oversized for many applications, especially for low-cost implementations.

While being a revolution in embedded system processor cores, RISC-V is now receiving increased interest for space and safety applications. In this work we illustrate a novel approach for developing robust Fault Tolerant RISC-V processor cores, using an Interleaved-Multi-Threading (IMT) architecture as a basis for Radiation Hardening technique, starting from an open-source RISC-V soft core family named Klessydra-T [2], developed at the Digital System's Lab group at Sapienza University of Rome, which interleaves three or more hardware threads in a round robin fashion on a four-stage in-order pipeline, and is fully compatible with the PULPino open-source microcontroller platform [3]. The basic concept of our work is the intrinsic FT capability of an IMT core running three threads, each having its own Register File (RF), Program Counter (PC) and Control/Status Registers (CSRs) incorporating *spatial redundancy,* yet sharing the pipeline logic and registers to execute the same instructions in different clock cycles, thus providing *temporal redundancy.* Contrary to FT approaches based on Simultaneous Multi-Threading (SMT) or Multi-Cores (MC) schemes [4], the proposed approach exploits the IMT scheme to merge spatial redundancy with temporal redundancy, leveraging specific logic structures to deal with the fact that the instruction results are not simultaneously available. Nevertheless, executing the instructions of identical threads on the same hardware in different clock cycles, protects the architecture from Single Event Upset (SEU) in sequential logic and from Single Event Transient faults (SET) that may occur in combinational logic. We call the proposed paradigm *Buffered TMR*, defining precise architecture modifications with general validity. The values produced by three harts in selected architectural units (PC, Register File, Write Back unit and Load Store Unit) are *buffered* in dedicated registers and voted at the end of each thread instruction cycle, by performing an intrinsic TMR protection and correct data retention. The obtained RISC-V processor core, named Klessydra-fT03 [1], possesses FT features briefly quoted in *Table 1* and validated by an extensive Fault Injection simulation campaign with Single-Event-Upset (SEU) faults targeting all the most used register bits in the architecture.

Table 1: Failure Probability (Pe %) averaged on the most used architectural bits with faults every 15 clock cycles.

benchmarks	**Klessydra-T03 (Pe%)**	**Klessydra-fT03 (Pe%)**
FFT	62 %	13 %
FIR	60 %	10 %

References

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