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Using the TUM Uncore Environment for RISC-V for Teaching, AI and Quantum Computing

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Abstract

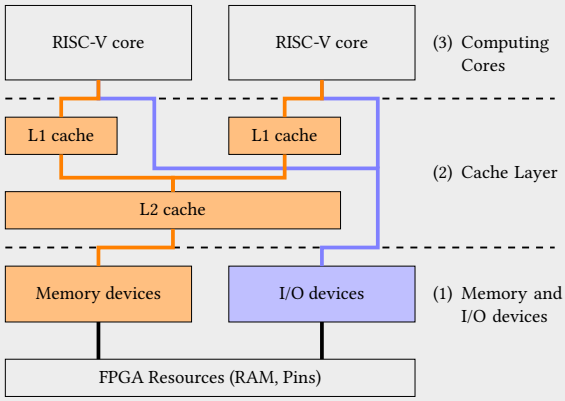
RISC-V is not only a good match for innovative research, from AI to Quantum Computing, but also for teaching and education. Both research and teaching with RISC-V are frequently conducted on FPGAs, as they offer a good trade-off between easy-to-implement simulations and high performance.

We have developed a small and simple, yet flexible and easy to use uncore environment to simplify the VHDL-based development of multi-core RISC-V processors from scratch on FPGAs. It forms the foundation for several activities at TUM, from core design in student labs, the development of new AI platforms to the research on quantum control processors.

The TUM Uncore Environment

Supported Functionality

- Support for multiple RISC-V cores
- Atomic operations to support multi-core communication
- Generic memory interface
- Configurable memory and cache latencies



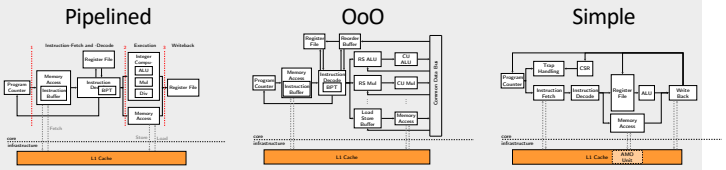
Layers of the TUM Uncore Environment

- Memory and I/O devices
- Optional cache layer(s) with coherence functionality
- Interface to compute cores

Connected via a bus-based communication protocol

Reference: Michael Jungmair, Tobias Schmidt, Alexis Engelke, Armin Eichenhofer, Felix Krayer, Jonas Lauer, Malte von Ehren, and Martin Schulz. 2021. A Flexible Uncore Infrastructure for RISC-V Core Development. In Proceedings of the Fifth Workshop on Computer Architecture Research with RISC-V (CARRV 2021)

Use Case 1: Student Labs



Three RISC-V Designs, One Infrastructure

- Developed in student lab projects
- Focus: 2nd semester bachelor students
- Ability to focus on design and not on the infrastructure

Part of the Intro Lecture on Computer Architecture (ERA)

Use Case 2: Environment for AI Chips

From Hardware Design to Chip Tape-Out

- New project to increase teaching of hardware designs
- Focus on AI accelerators
- Paired with RISC-V CPUs
- Target application: image processing for drones

Easier Ramp-Up with Uncore Support

- Integration of existing RISC-V designs
- Shared global memory
- Easier testing and validation
- Focus on AI designs during development

Part of the BB-KI Chips Project

Use Case 3: Quantum Control Processors

Quantum Computers Need Conventional Control

- Interfaces with existing systems
- Laser/microwave (or similar) control
- Read-out and evaluation

New Concepts Needed to Drive Control

- New ISAs to encode quantum operations
- Goal: pairing with RISC-V designs
- Common substrate will support development and use of new chip architecture
- Going beyond von-Neumann to support QPUs?

Part of the Munich Quantum Valley Project (MQV)

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