Pipeline Datapath Models from RISC-V based cores
Samira Ait Bensaid, Mihail Asavoae, Farhat Thabet and Mathieu Jan
Université Paris-Saclay, CEA, List, F-91120, Palaiseau, France
samira.aitbensaid@cea.fr, mihail.asavoae@cea.fr, farhat.thabet@cea.fr, mathieu.jan@cea.fr

Motivation

• Safety-critical systems rely on the use of timing analyses under architecture considerations to estimate Worst-Case Execution Times (WCET).
• Such architecture models generally built by hand in WCET analyzers, while using the open hardware frameworks [2] its automation could be possible.
• Generating hardware models for timing analysis have Verilog/VHDL designs [3]. However, hardware designers tend to use higher-level and more expressive languages, such as Chisel.

Contributions

• Automatic construction of datapath pipeline model from high-level hardware designs [1].
• Evaluation of the approach on in-order RISC-V processors.

Experimental results on RISC-V processor designs

An application of the analysis on a set of in-order RISC-V processors: 3 to 5 stages.

<table>
<thead>
<tr>
<th>LOC</th>
<th>#Regs</th>
<th>Rule 1</th>
<th>Rule 2</th>
<th>#Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>RISC-V Mini</td>
<td>241</td>
<td>15</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Sodor</td>
<td>646</td>
<td>48</td>
<td>34</td>
<td>14</td>
</tr>
<tr>
<td>KyogenRV</td>
<td>4567</td>
<td>93</td>
<td>47</td>
<td>36</td>
</tr>
</tbody>
</table>

Perspectives

• Develop an extended analysis for multi-modular datapath pipelines and out-of-order processors.
• Generate the abstract formal models to verify timing properties.

Illustration on RISC-V SODOR 5-stages processor


Pipeline datapath analysis

• Pipeline analysis algorithm:
  - Identified the processor registers.
  - Explore the combinatorial and sequential logics to build the registers context.
  - Build the dependency relations between registers.
  - Assign to each register its pipeline stage based on two rules:
    • Rule 1: register dependencies.
    • Rule 2: based on a heuristic "when" conditional block.
  - Deduce the pipeline depth and construct the pipeline datapath model.

Bibliographie