whISPer: Enhancing MemPool to Make an Open and General-Purpose Image Signal Processor

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To tackle the large computational loads of multimedia applications, specialized platforms called image signal processors (ISPs) have been developed to meet the demanding requirements of power- and timing-constrained environments thanks to their highly-parallel architectures and domain-specific instructions. However, such state-of-the-art systems are often tied to specific algorithm families, exhibit low programmability, or are not open to the community. MemPool is a novel 32-bit many-core general-purpose system with 256 cores sharing a L1 scratchpad memory pool through a low-latency interconnect [1]. Each core is implemented by a RV32IMA Snitch: a tiny, efficient, and flexible processor based on the RISC-V open instruction set architecture (ISA), paired with an application-tunable accelerator.

Until now, the term ISP has been referring to highly-specialized closed-source architectures. In this work, we close the gap between power- and time-efficient image processing and general-purpose capabilities, while keeping high bare-metal programmability and an open-source nature. In particular, we present *whISPer*, a domain-specific accelerator implementing selected digital signal processing (DSP) instructions from the Xpulp custom RISC-V extension [2]. These include single-instruction-multiple-data (SIMD) operations, new addressing modes for load and store instructions, and additional arithmetic utilities for DSP. We couple each one of the 256 Snitch cores to a whISPer, to exploit the parallelism and the general-purpose architecture of the MemPool cluster. To fully support this extension and make it compliant with the open, modular, and extensible character of the standard RISC-V ISA, we also propose a complete framework for opcode space management, ISA modeling and simulation, verification, and compilation support, based on the tools provided by RISC-V International.

To make the most out of the extended ISA, we develop optimized computational kernels for matrix multiplication and convolution, which we employ to evaluate the proposed extension. The benchmarking of the whole MemPool cluster shows a speed-up of up to 4.6× with respect to the baseline design. Post-synthesis figures, very much taken into account for the micro-architectural design exploration, are collected from the modern GlobalFoundries' 22FDX Fully-Depleted Silicon-Over-Insulator (FD-SOI) technology and demonstrate an energy efficiency 3.8× higher at the MemPool-tile level.

References

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