whISPer: Enhancing MemPool to make an Open and General-Purpose Image Signal Processor

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The challenge

- Computer vision
- Augmented reality
- Computational photography
- …and many more

- High computational load
- Real-time constraints
- Tight power envelope

- High data parallelism
- Domain-specific processing

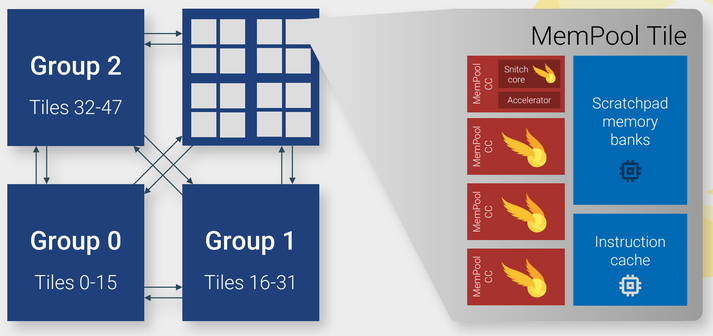
Image Signal Processors (ISPs)

\+ Highly parallel architectures
\+ Domain-specific instructions

gap

\- Domain-specific processing models
\- Closed source

The playground: MemPool & Snitch



- Highly parallel (256 `rv32ima` Snitch cores)
- Efficiently solves L1 cache sharing
- General-purpose
- High bare-metal programmability
- Open-source

CONTRIBUTIONS

1. Snitch DSP ISA extension: **whISPer** accelerator for efficient image processing in MemPool
2. Open-source **framework for Snitch ISA extensions** development and support

Closing the **gap**: parallel, general-purpose, open-source, time- and power-efficient image processing

1. Snitch ISA DSP extension & whISPer accelerator

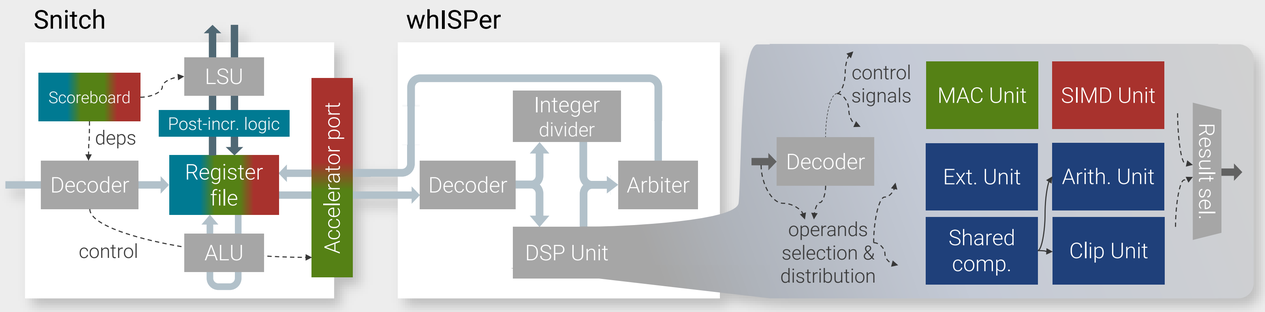
Selected instructions for *image processing*; implementation optimized for **area/performance**, targeting massive *replication* in MemPool

Extended generic arithmetical operations
- Comparisons, min, max
- Absolute value
- Sign/zero-extension
- Clip operations

Extended load/stores addressing modes
- Post-increment load/store instructions
- Load/store instructions with register offset

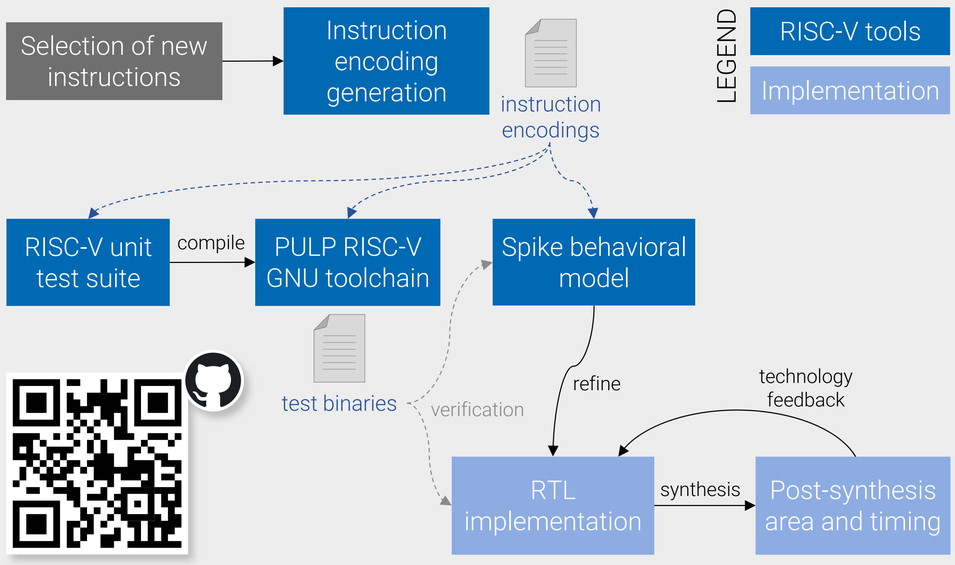
Multiply-accumulate operations
- Multiply & accumulate
- Multiply & subtract

8-bit and 16-bit packed SIMD
- Dot-product
- Logical & arithmetical ops
- Shift operations
- Packing, unpacking, shuffle



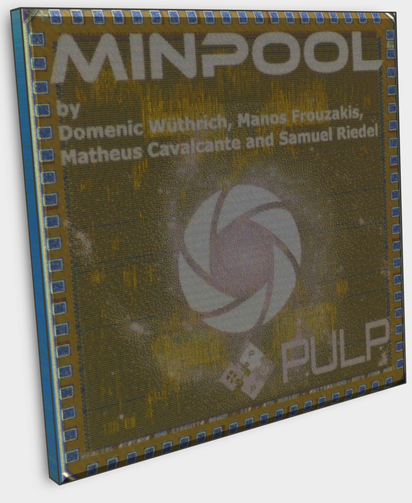
2. Supported by an open-source framework

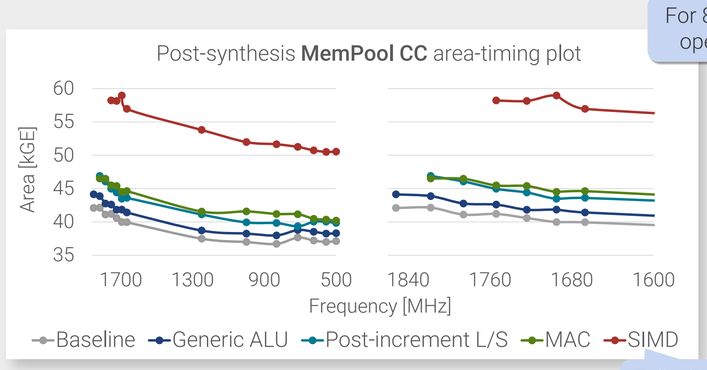
Based on **RISC-V tools**; supports *whISPer ISA*, simplifies *further extension* and *design exploration*

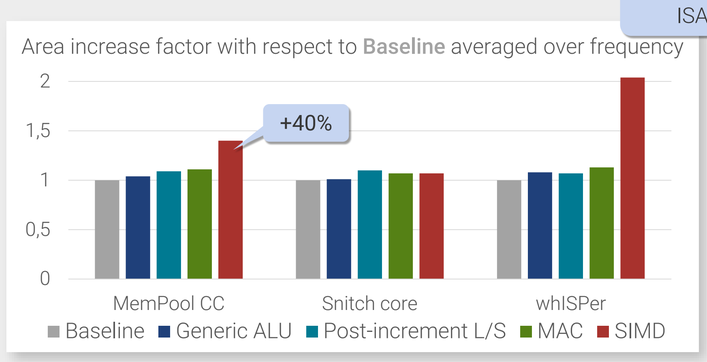


Results

whISPer makes MemPool up to **4.6x faster** and **3.8x more energy efficient**

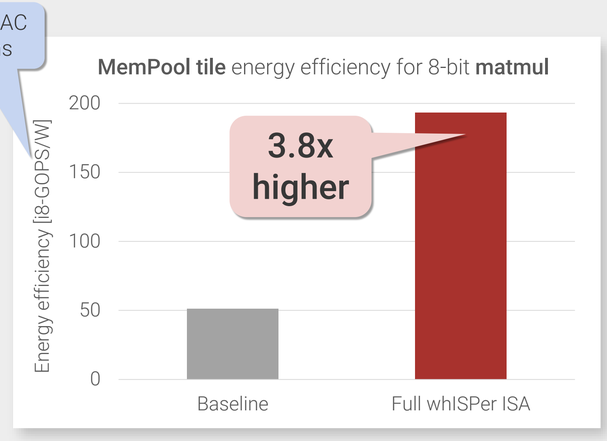


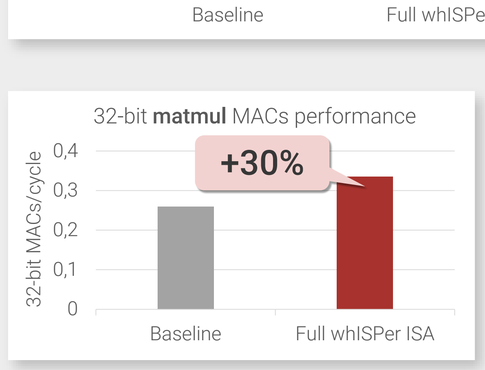


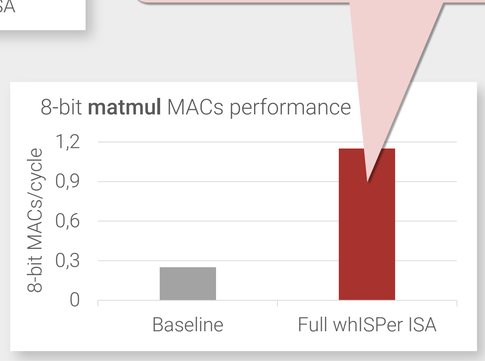


For 8-bit MAC operations

Full whISPer ISA







- **4.6x more MACs/cycle**
- ~same amount of instructions
- **IPC** from 0.93 to **0.97**

◀ exciting, right? find out more!

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