Comet: a RISC-V Core Synthesized from C++ Specifications

Simon Rokicki, Joseph Paturel, Olivier Sentieys

Univ Rennes, Inria, IRISA - Rennes, France

{simon.rokicki, joseph.paturel, olivier.sentieys}@irisa.fr

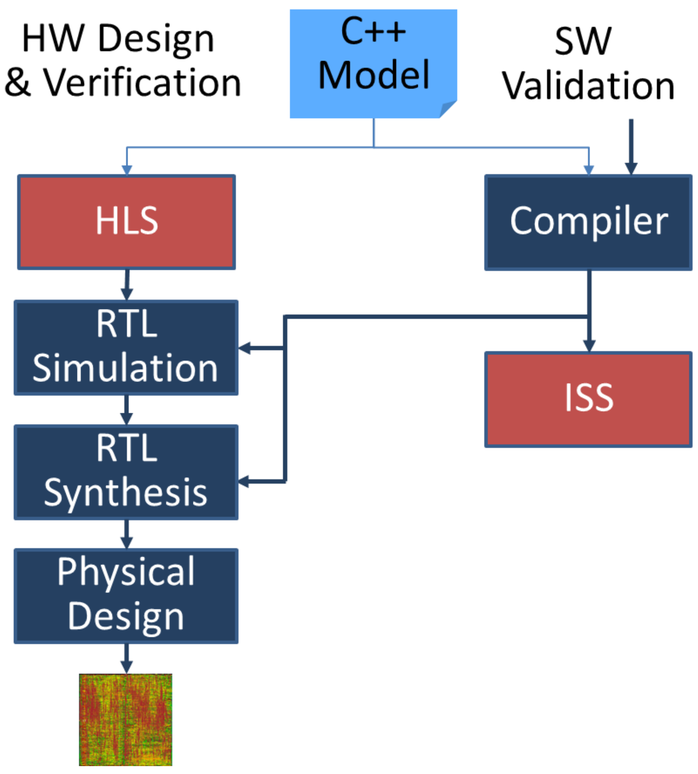
Introduction

Designing the hardware of a processor core as well as its verification flow from a single high-level specification would provide great advantages in terms of productivity and maintainability.

In this work, we highlight the gain of starting from a unique high-level synthesis and simulation C++ model to design a processor core implementing the RISC-V ISA

Development flow

What you simulate is what you synthesize



Current Project Status

Current project features:

- Specification of 5-stage pipelined RISC-V core for rv32i or rv32im
- Configurable cache architecture
- Support for Zephyr OS
- Simple SoC for Artyx-7 FPGAs
- Simple to use and to modify
- Already used in several research projects

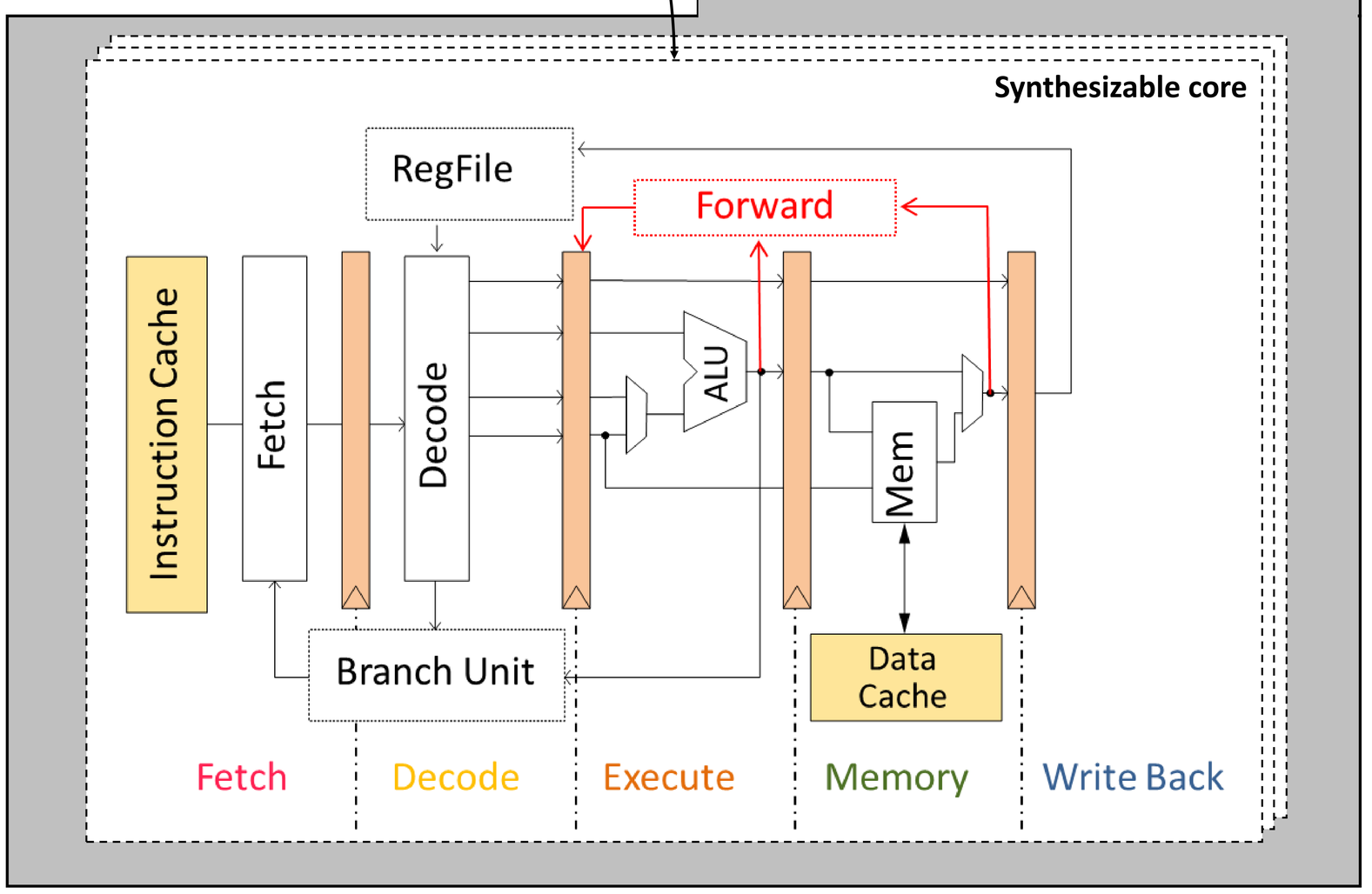
Pipelined architecture and simulator

```
struct FtoDC ftodc;
struct DCtoEx dctoex;
struct ExtoMem extomem;
struct MemtoWB memtowb;
while true do
   ftodc_tmp = fetch();
   dctoex_tmp = decode(ftodc);
   extomem_tmp = execute(dctoex);
   memtowb_tmp = memory(extomem);
   writeback(memtowb);
   bool forward = forwardLogic();
   bool stall = stallLogic();
   if (!stall) then
      ftodc = ftodc_tmp;
      dctoex = dctoex_tmp;
      extomem = extomem_tmp;
      memtowb = memtowb_tmp;
   end
   if forward then
      dctoex.value1 = extomem.result;
   end
end
```

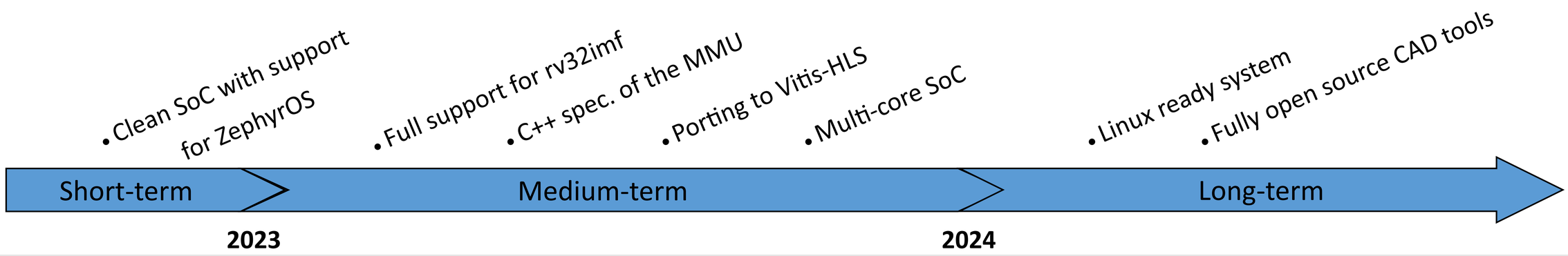
HLS

Simulation Environment

- Instrumentation
- Syscall emulation
- Elf reader
- Not-yet Synthesized extensions
- L2 cache
- Shared cache policy
- Multi-core system



Development Roadmap



Conclusion

The Comet project highlights the benefits of using HLS to develop CPU cores since it significantly reduces development and debugging time. Experimental studies show that the generated core has an area comparable with cores developed using standard development flows.

References

Simon Rokicki, Davide Pala, Joseph Paturel, Olivier Sentieys. What You Simulate Is What You Synthesize: Designing a Processor Core from C++ Specifications. ICCAD 2019 - 38th IEEE/ACM International Conference on Computer-Aided Design, Nov 2019, Westminster,

Get started at: https://gitlab.inria.fr/srokicki/Comet