RISC-V week Introduction

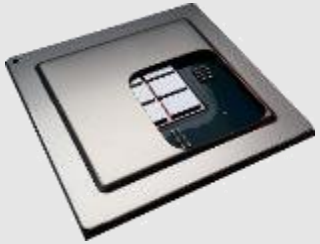
DE LA RECHERCHE À L'INDUSTRIE

3rd, may 2022

Fabien CLERMIDY, PhD

Welcome to a real event!

Nanoelec Technology Research Institute



Innovative components, systems and processes, for electronics industry

Technology dissemination

Human Capital & training engineering

Nanoelec Technology Research Institute

Key figures

- 22 members
- Average Annual Budget 54 M€
- 214 equivalent Full time jobs in 2021
- 224 patents and 46 software solutions filled since 2012
- 544 publications since 2015
- 295 associated partners (inc. 218 SME) since 2012

Current scientific themes

Images & Photons

Smart Imagers, Displays

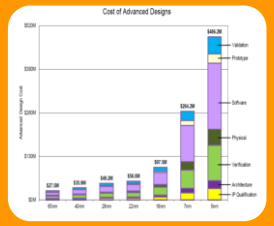
Photonic sensors

Digital Trust

IOT & cybersecurity for embedded components & systems

Characterization of components & systems

Semiconductor general context



More performance / less power paradox

- Exploding design costs of advanced nodes
- Specialization required for power consumption

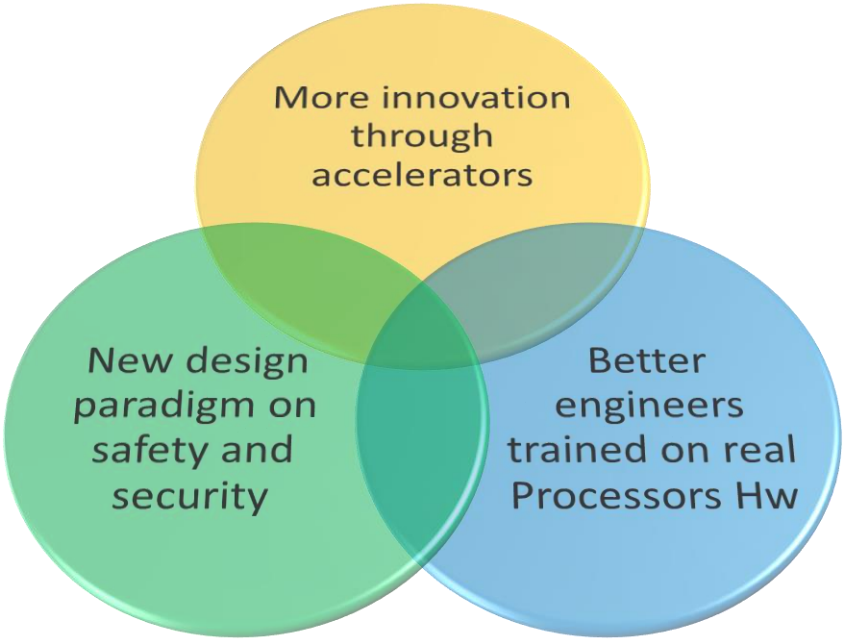
Embedded & critical

- Safety
- Security

Designer shortage

- Training
- Community

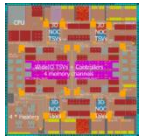
RISC-V & OpenHw opportunities



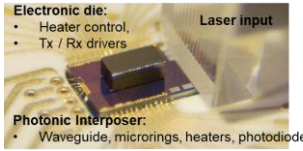
HORIZON-KDT-JU-2021-1-IA - Focus Topic 1: Development of open-sources RISC-V building blocks

RISC-V is getting momentum in our chips developments

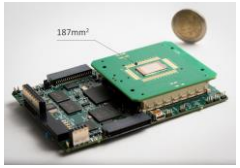
High-performance



MAG-3D
3D Network-on-Chip



HUBEO
Photonic NoC interposer



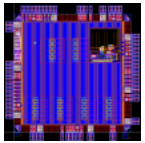
RETINE
Ultra-fast smart imager

INTACT
6 chiplets & 96 processors

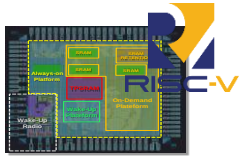
EPAC
HPC Variable Precision Accelerator

Low-power

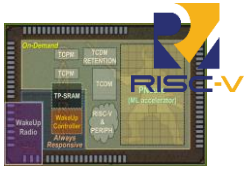
LOCOMOTIV
Adaptive Voltage & Frequency Scaling



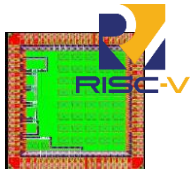
FRISBEE
ULP FDSOI demonstrator



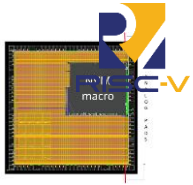
WARRIOR
RISC-V IoT IC with wake-up



SAMURAI
IoT IC with NN accelerator

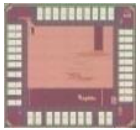


Cyber-VT
Test Vehicle for IoT security enhancement

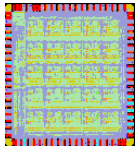


Non-Volatile-Memory
NVM subsystem for Microcontrolers

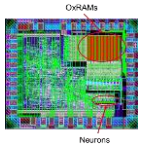
New concepts



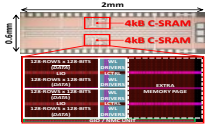
REPTILE
Analogue neuron



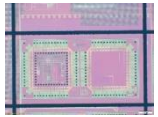
SPIDER
Neuromorphic DSP



SPIRIT
Spiking NN with eNVM



In-Memory-Computing
Compute-SRAM



CRYOCMOS
Control for quantum computing

ESPERANTO
RNN with 50k synapses

2011 2021

VR/XP: VaRiable eXtended Precision RISC-V Accelerator

Hardware RISC-V accelerator enabling computations with Variable and eXtended Precision Floating-Point (FP) numbers.

Why another hardware accelerator ?

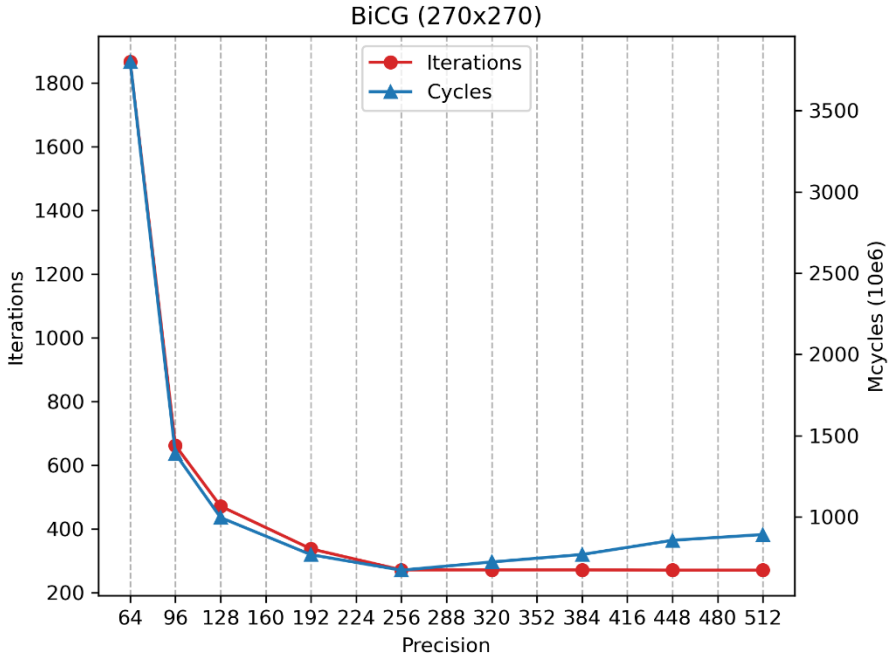
Native hardware support for arithmetic and memory operations enables much higher performance than software-based approaches **(up to x835 speedup)**

Why variable precision (VP) ?

Allows to tailor the data format to the needs of the application. This reduces both latency and memory footprint.

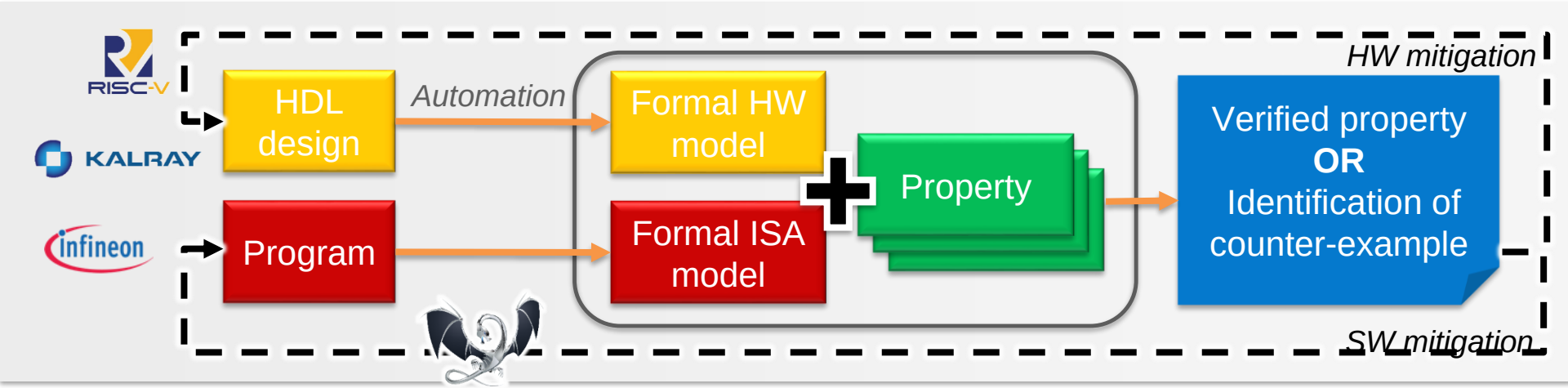
Why extended precision ?

Allows the solver to converge faster (it reduces the number of iterations)



LEAF: formal analysis of HW/SW processing

- **Verifying timing properties requires to encompass both SW+HW**
  - Safety property: code-specific detection of timing anomalies within pipelines of processors
  - Security property: identification of fault-injection points in a µ-architecture that lead to SW exploits

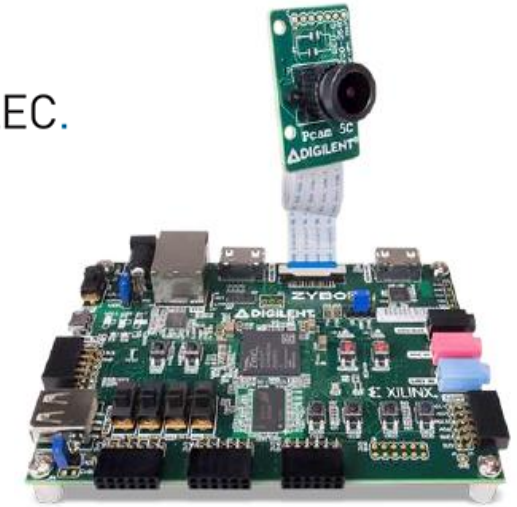


- **LEAF: combine both HW and SW formal models in the analysis**
  - Use of formal methods (model-checking / static analyses)
  - Based on HDL design or timing specification
  - Towards mitigation solutions: SW (compilation) and/or HW (e.g. flex. arbitration policies)

Education & Training

- Training Modules RISC-V for embedded systems @Grenoble-INP
  - GINP/Phelma: Integrated Digital Systems
    - module « Design project of an integrated system »
  - GINP/Phelma & Ensimag: Embedded Systems & Smart Objects (IOT)
    - module « Embedded system project »

- **Prepare future engineers to use the platform Risc-V .**
- **Design a semi-generic reference platform for teaching by developing basic units**
  1. Design of FPGA embedded vision systems
  2. AI based applications (neuronal networks CNN).
- **Involving students on generic projects**
  1. With educational demonstrator
  2. Reference design environment, user manual



Enjoy the event!