



Spring 2022 RISC-V Week

Paris



Tuesday 3<sup>rd</sup> to Thursday 5<sup>th</sup> May 2022

# Overview of the “Spring 2022 RISC-V Week” and “4th RISC-V Meeting”

Christian Fabre (CEA LIST, IRT-Nanoelec)  
May 3<sup>rd</sup>, 2022 – Paris



# “RISC-V Week” and “RISC-V Meeting” Series

## Previous Editions

- Oct. 2018, at CEA Grenoble
  - 1st RISC-V Meeting, single day
- Oct. 2019, Paris – 1st RISC-V Week
  - 2nd RISC-V Meeting, two days
  - 1 day by CNRS' GdR SOC2
- Mar. 2021, online from Rennes
  - 3rd RISC-V Meeting, two days
  - 1 day by OpenHW Group

## Spring 2022 RISC-V Week – On-line, on-site

- May 3-4: 4th RISC-V Meeting
- May 5: RISC-V International Day





# Spring 2022 RISC-V Week

## Format, sponsors, organizers

### Keep and extend the format

- Still the 2+1 days format:
  - 4th RISC-V Meeting
  - RISC-V International Day
- Poster session, with CfP
- Exhibition and booths
- Social event, to resume networking after 2 years of pandemics!



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**THALES**



**SIPEARL**

**E4** | COMPUTER  
ENGINEERING







# 4th RISC-V Meeting

## First day: Tuesday May 3rd

08h00	Registration, distribution of badges.	
09h00	Fabien Clermidy	Welcome Address from the IRT NanoElec
09h15	Christian Fabre	Overview of the “Spring 2022 RISC-V Week”, “4th RISC-V Meeting”
09h25	Kevin Martin	Introduction to the posters sessions
09h30	Frédéric Pétrot	Tutorial host
09h30	Alistair Francis	Free RISC-V Systems: Benefits, Status of QEMU
10h15	Break – exhibition, first poster session are open	
10h45	Teresa Cervero	Session on the RISC-V Software Stack
10h45	Nick Kossifidis	Demystifying the RISC-V Linux software stack
11h30	Roger Ferrer	SW Toolchain for RISC-V Vector Extensions
11h50	Teresa Cervero	Panel with Nick, Roger on the RISC-V Software Stack
12h00	Marion Andriolat	Session on the exhibition
12h00	Introduction of the booths of OpenHW Group, SiFive, CodaSip, Andes Technology, Siemens, RISC-V International, CEA	
12h30	Lunch – exhibition, first poster session are open	

12h30	Lunch – exhibition, first poster session are open	
14h00	Jérôme Quévremont	Session on RISC-V in practice
14h00	Michael Gielda Adam Jesionowski	Springbok: Using Renode, IREE to prototype, develop ML models on RVV
14h30	Mathieu Jan	Formal Processor Modeling for Analyzing Safety, Security Properties on RISC-V case studies
14h45	Borja Pérez	Coyote: an open-source simulator for HPC architectures
15h00	Andrea Bartolini	RISC-V based Power Management Unit for an HPC processor
15h30	Jérôme Quévremont	Panel with Michael, Mathieu, Borja,, Andrea on RISC-V in practice
15h45	Break – exhibition, first poster session are open	
16h15	Maxime Pelcat	Session on EDA tools
16h15	Jean-Roch Coulon	Verification of the CVA6 Open-Source Core
16h45	Jan Kuper	Digital hardware design with Clash
17h15	Luca Carloni	Open-Source Hardware for Heterogeneous Computing with ESP, RISC-V
17h45	Maxime Pelcat	Panel with Jean-Roch, Jan,, Luca on EDA tools
18h00	End of 1st day of the “4th RISC-V Meeting”	



# 4th RISC-V Meeting

## Second day: Wednesday May 4th

<b>08h30</b>	<b>Registration, distribution of badges.</b>	
09h00	Olivier Sentieys	Keynote Host
09h00	Rick O'Connor	Open-Source HW Commercial Adoption: Lessons Learned
09h45	Sébastien Pillement Jérôme Quévremont	French RISC-V Student Contest: Lessons Learned
<b>10h00</b>	<b>Break – first poster session (last time), exhibition are open</b>	
10h30	Romain Dolbeau	Session on the European Processor Initiative (EPI)
10h30	Jesús Labarta	The Accelerator Tile of European Processor Initiative
11h00	Francesco Minervini	Vitruvius: An Area-Efficient RISC-V Decoupled Vector Accelerator for High Performance Computing
11h15	Matheus Cavalcante	The RISC-V based Stencil Tensor Accelerator of EPI
11h30	César Fuguet Tortolero	VRP/VXP: VaRIable eXtended Precision RISC-V Accelerator for High-Precision
11h45	Romain Dolbeau	Panel with Jesús, Francesco, Matheus, César on the EPI
<b>12h00</b>	<b>Lunch – second poster session, exhibition are open</b>	

<b>12h00</b>	<b>Lunch – second poster session, exhibition are open</b>	
13h30	John Davis	Session on RISC-V computing cores
13h30	Olof Kindren	How much score could a CoreScore score if a CoreScore could score cores?
13h50	Roger Espasa	Atrevido: SemiDynamics Out-of-Order RISC-V Core
14h10	Charles Papon	NaxRiscv: An open-source OoO superscalar softcore
14h25	Zdeněk Přikryl	Customizing RISC-V designs to unlock innovation with CodaSIP
14h40	Davide Schiavone	OpenHW CORE-V Roadmap
14h55	Jérôme Quévremont	An Open-Source Application Core: CVA6 from the OpenHW Group
15h10	John Davis	Panel with Olof, Roger, Charles, Davide, Jérôme on RISC-V computing cores
<b>15h45</b>	<b>Break – second poster session, exhibition are open</b>	
16h00	Olivier Savry	Session on CHERI
16h00	Simon W. Moore	Intro to CHERI capability-based memory protection
16h30	Jonathan Woodruff	The CHERI-RISC-V experimental extension
16h45	Peter Rugg	Four CHERI RISC-V micro-architectures
17h00	Alex Richardson	Software Ecosystem: QEMU, LLVM, CheriBSD
17h15	Franz Fuchs	Demo: Detecting, Resolving an Exploit under CheriBSD on a Multi-core, Superscalar Softcore
17h30	Olivier Savry	Panel with Simon, Jonhathan, Peter, Alex, Konrad on CHERI.
18h00	Christian Fabre	Session on more fun to come at the “Spring 2022 RISC-V Week”!
18h00	Calista Redmond	Introduction, program of the “RISC-V International Day”
18h10	Christian Fabre	Closing remarks for the “4th RISC-V Meeting”, timing, directions to the diner cruise
<b>18h15</b>	<b>End of 2nd, last day of the “4th RISC-V Meeting”</b>	



# RISC-V International Day

## Thursday May 5th

08h30 Registration, distribution of badges.

09h00	Mark Himmelstein	State of the Union & the Road Ahead
09h30	Philipp Tomsich	Driving Innovation: Evolving the Role of Software in the RISC-V Ecosystem Beyond Enablement
09h50	Philipp Tomsich Mark Himmelstein	Maturing the RISC-V Ecosystem: From Technology to Product

10h15 Break – second poster session, exhibition are open

10h45	Johanna Baehr	Open Source IC Design, Hardware Reverse Engineering Or: How I Learned to Stop Worrying, Love Reverse Engineering RISC-V Designs
11h05	Calista Redmond	Global Importance, Adoption, Opportunity for Europe in RISC-V
11h35	Florian Wohlrab	RISC-V Goes Big
11h55	Andrew Dellow	RISC-V : Securing the Future of Open Source Computing

12h20 Lunch – second poster session, exhibition are open

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13h50	Jérôme Quévremont	Introduction to RISC-V Functional Safety Special Interest Group
14h10	Perrine Peresse	RISC-V IOMMU Architecture Overview
14h30	Olof Kindgren	CPU is Only as Good as its Ecosystem: Turning RISC-V CPUs into Systems with FuseSoC

14h55 Break – second poster session, exhibition are open (last time for both)

15h25	Gary Martz	Intel Investment to Help Deliver a Thriving RISC-V Ecosystem
15h45	John Davis	Building an Open HPC Ecosystem
16h05	John Hartley	RISC-V Compatible Processor IP by Syntacore
16h25	Michael Gielda	Unlocking Open Source RISC-V SoC Verification
16h45	Calista Redmond Christian Fabre	Closing Remarks

17h00 End of the “RISC-V International Day”, of the “Spring 2022 RISC-V Week



# Posters

## First session

- Already started
- Tuesday 3rd
  - Morning break
  - Lunch
  - Afternoon break
- Wednesday 4th
  - Morning Break
  - Ends after morning break

## Second session

- Wednesday 4th
  - Starts after the morning break
  - Lunch
  - Afternoon break
- Thursday 5th
  - Morning break
  - Lunch
  - Aftrenoon
  - Ends after afternoon break

Spring 2022 RISC-V Week

Paris



Tuesday-Thursday

May 3-5

7 booths



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**SIEMENS**







# Social Event

## Dinner-cruise on the Seine



- **19h30:** Boarding on Le Saphir begins at Port de la Tournelle.
  - **20h00:** End of boarding. Le Saphir leaves the port. Start of the cruise.
  - **20h30:** Dinner begins – buffet
  - **23h00:** Le Saphir returns to the port. Unboarding starts.
  - **00h00:** End of the party. The last guests shall leave the boat.
- 
- The port is at a 15 min. walk from the conf. center
  - Please be on time
  - More details tomorrow, with flyers



# Miscellaneous

- The program is online and printed as posters, with abstracts
- For most sessions, Q&A will be a mini panel after the last speaker
- There is a ~45 sec. lag for online audience
  - Online audience: please ask questions in the chat during the talk
- Breaks will last 30 min.
- Lunches will be 90 min. buffet
- Take time to visit posters and booths
- Lots of room on the terraces above for private discussion
- Lots of electrical outlets behind your feet
- WiFi – one access per attendee:
  - SSID is « CONGRES »
  - Login is « RISC-V?? » to each his/her own
  - Password is « ●●●●● » to each his/her own
- No food nor drinks in the amphitheater



Thanks to our sponsors and organisers

