Posters - Spring 2022 RISC-V week

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Submissions

(light) Submission format

One page abstract in pdf

Selection

38 submissions - 38 accepted posters

2 sessions

1. starts on Tuesday May 3 at 09h00, and will last until Wednesday 4 at 10h30 - the end of the morning break
2. starts sometime after the same morning break on Wednesday 4 at 10h30, and will last until the afternoon break on the Thursday May 5, at 15h30.

Topics and Partitioning

11 categories - set by the members of the committee

1. Memory hierarchy
2. Security
3. Core extensions and optimizations
4. SoC design
5. SoC or Core Performance evaluation
6. Design automation and CAD
7. Educational systems
8. Multi/many-core
9. Application-specific or domain-specific architectures
10. Fabrication and prototype
11. Safety and error resilience

A balance between the categories and constraints from the presenters

1. 19 posters: 1×C1, 2×C2, 3×C3, 2×C4, 2×C5, 1×C6, 1×C7, 5×C9, 1×C10, 1×C11
2. 19 posters: 4×C2, 3×C3, 3×C4, 3×C5, 1×C6, 2×C9, 1×C10, 1×C11

Session 1

1. A memory hierarchy protected against Side-channel Attacks
2. Variability-aware Deep Sub-micron Low- energy Designs for IoT RISC-V Processors
3. Implementing Functional Safety in a RISC-V Interleaved-Multi-Threading Processor Core
4. Formal Analysis of Fault Injection Effects on RISC-V Microarchitecture Models
5. SCI-FI: Control Signal, Code, and Control Flow Integrity against Fault Injection Attacks
6. A RISC-V VPU for Very Long and Sparse Vectors
7. MINOTAuR: A Timing-Predictable Open Source RISC-V Core Featuring Speculative Execution
8. RISC-V Virtualization for a CVA6-based SoC
9. A RISC-V Heterogeneous SoC for Embedded Devices
10. Enabling RISC-V in Large Scale FPGA Platforms
11. Comet: a RISC-V Core Synthesized from C++ Specifications
12. Pipeline Datapath Models from RISC-V based cores
13. Direct Convolution: Performance Effects of Loops Ordering and Parallelization
14. RVfpga: Understanding - Computer Architecture
15. Accelerating applications with RISC-V Systolic Array Coprocessors
16. An Application Specific Processor for CNN-Based Massive MIMO Positioning
17. An Energy-Efficient Near-Memory Computing Architecture for CNN Inference at Cache Level
18. Energy-Efficient Application-Specific Instruction-Set Processor for Feature Extraction in Smart Vision Systems
19. Open Hardware for Near-Sensor Signal Processing and Machine Learning

Session 2

1. Meet Monte Cimone: Exploring RISC-V High Performance Compute Clusters
2. Experimental evaluation of neutron-induced errors on a RISCV processor
3. An open CAD flow to optimised key gate insertion in logic locking
4. Insertion of random delay with context-aware dummy instructions generator in a RISC-V processor
5. Noise-Free Security Assessment of Eviction Set Construction Algorithms with Randomized Caches
6. Towards Low-Power and Low Data-Rate Software-Defined Radio Baseband with RISC-V Processor for Flexibility and Security
7. Arbitrary and Variable Precision Floating-Point Arithmetic Support in Dynamic Binary Translation
8. Automatic RISC-V Processor Synthesis using Speculative Pipelining
9. Composable Custom Extensions and Custom Function Units for RISC-V - *available online*
10. Deterministic Cache Coherent ManyCore Environment for Embedded Systems
11. Using the TUM Uncore Environment for RISC-V for Teaching, AI and Quantum Computing
12. whISPer: Enhancing MemPool to Make an Open and General-Purpose Image Signal Processor
13. Graph Analytics on RISC-V GPU: Where are the Bottlenecks?
14. Removing Load-use dependencies bottleneck from CVA6 application class core
15. Towards the next generation Heterogeneous Multi-core Multi-accelerator Architectures for Machine Learning
16. Agile Design Methodology for Accelerator-Rich Cluster-based RISC-V SoC
17. ControlPULP: A Multi-Core RISC-V Power Controller for HPC Processors
18. RISC-V based Embedded Systems For Always-on Energy Efficient Smart Sensing with TinyML
19. Specialized Scalar and SIMD instructions for Error Correction Codes Decoding on RISC-V processor

Enjoy

Abstracts and posters on the website

`https://open-src-soc.org/2022-05/posters.html`
Available as long as possible

Message to poster contributors

If not already done, please send your poster to
webmaster@open-src-soc.org
No obligation though

Thank you

... and thanks to the presenters and contributors

... and sorry to the people online