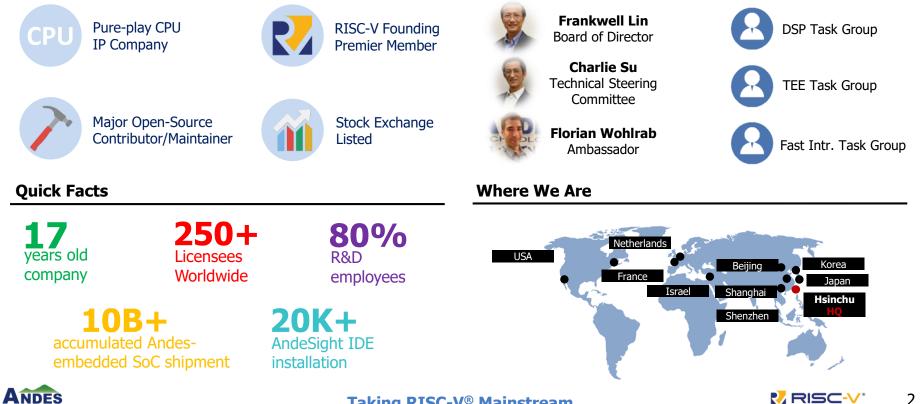
ANDES TECHNOLOGY

Florian Wohlrab Sales Manager EMEA & Japan Andes Technology

ROL

Company Profile

Who We Are



Taking RISC-V® Mainstream

Roles in RISC-V International

2

Innovation on Open Architecture

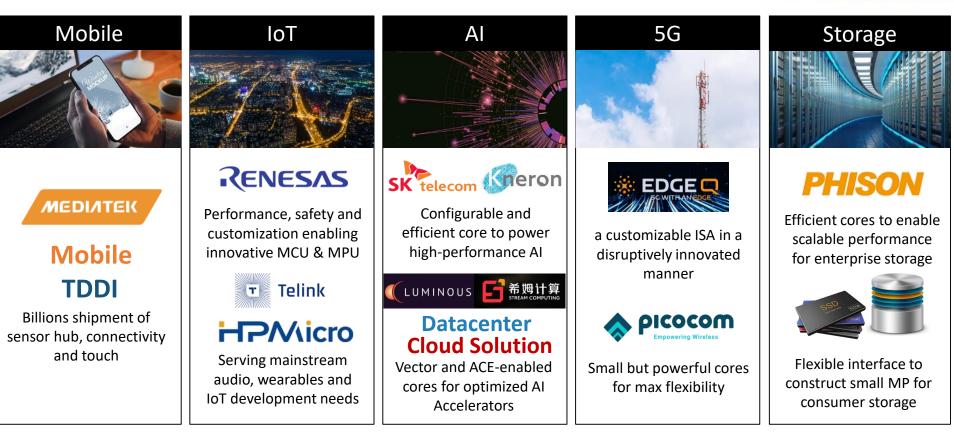




Taking RISC-V® Mainstream



Powering World-Leading SoC Customers





Taking RISC-V® Mainstream

Renesas 64-bit RISC-V General-Purpose MPU

Pioneering RZ/Five General-Purpose MPUs with 64-Bit RISC-V CPU Core



RZ/Five Block Diagram

			N	
NE	RZ/Five	RZ/G2UL	RZ/G2LC	RZ/G2L
Main CPU	64-bit RISC-V x1	Cortex-A55 x1	Cortex-A55 x2 or x1	Cortex-A55 x2 or x1
Sub CPU	-	Cortex-M33 x1	Cortex-M33 x1	Cortex-M33 x1
Gigabit Ethernet	2ch or 1ch	2ch	1ch	2ch
CAN-FD	2ch	2ch	2ch	2ch
12-bit ADC	2ch	2ch	-	8ch
Package	13mm Square BGA * 11mm Square BGA	13mm Square BGA *	13mm Square BGA	15mm Square BGA 21mm Square BGA

----- Pin Compatible ------*



System	CPU	
Debugger	AX45MP Single (1GHz)	
16ch DMAC	With SIMD / FPU I-L1\$: 32KB, D-L1\$: 32KB	
Interrupt Controller	TCM(ILM/DLM) :Total 128KB (1GHz)	
PLL/SSCG	L2\$:256KB	Ŀ
		н
Timers	Internal Memory	
1 x 32bit MTU3	SRAM: 128KB	E
8 x 16bit MTU3		
1 x WDT	Security	
	Secure Boot	
	Crypto Engine	
Analog	Secure JTAG	
2 input 12-bit ADC (1 unit)	TRNG	С
Thermal Sensor	OTP 1Kbit	





* : The 266pin package has one channel of Gigabit Ethernet.

Package Information : 361pin, 13x13mm PBGA (0.5mmPitch) 266pin, 11x11mm PBGA (0.5mmPitch)

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RISC-V the future is here now!

Thank You !



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