Technological research, catalyst and accelerator of innovation serving industry

May 2022
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CEA INTRODUCTION

Defense

Low carbon energies

Technological Research for Industry

Fundamental research

Most innovative organisations

1st European

3rd global

CEA

May 2022
4,500 employees

4 Institutes

- LETI: Semiconductor technologies, IOT, medical devices
- LITEN: New technologies of energy
- LIST: CPS, data intelligence, manufacturing
- French Regions: platforms within French regions

Budget

€625 Million/year

- 25% basic government funding
- 75% industrial income

600 patents/year

- 750 covering the CEA as a whole
  ~ 400 patent families covering international markets
  - The leading World player for research (INSEAD-WIPO)
  - The leading French player for PCT patent applications
600 industrial partners
15% international
Bring your digital IP block for assessment, RISC-V Silicon Starter is a one-stop shop IC test vehicle to move it to silicon

- More than 6 years of experience in RISC-V System on Chip design
- Pioneer in FD-SOI technologies & Ultra Low Power Design
- Industrial equipment from emulation to test
- Cybersecurity focused design teams (large patent portfolio)
- State-of-the-art cybersecurity characterization teams & tools
a RISC-V Computing Accelerator Designed for High Precision Computation (up to 512 bit mantissa)

Dedicated hardware/software accelerator suitable for the resolution of large ill-conditioned systems of equations. Its tunable, dynamic precision speeds up convergence and improves memory usage and computational efficiency.

The VXP accelerator supports arithmetic operations in hardware with up to 512 bits of mantissa. Its dynamic precision is fine grain tunable for optimal use of near processor memory.

- Silicon proven in GF 22nm FDX, new design in TSMC 7nm (European Processor Initiative)
- FPGA board for early access
- C-like programming environment (compiler and assembler)
- Library for mathematic and low-level algebraic subroutines
- Runtime environment
Formal Processor Modeling for Analysing Safety and Security Properties on RISC-V case studies
Mathieu Jan
Tuesday – 14h30

VRP/VXP: VaRiable eXtended Precision RISC-V Accelerator for High-Precision
César Fuguet Tortolero
Wednesday – 11h30

SCI-FI: Control Signal, Code, and Control Flow Integrity against Fault Injection Attacks
Formal Analysis of Fault Injection Effects on RISC-V Microarchitecture Models
Pipeline Datapath Models from RISC-V based cores
A memory hierarchy protected against Side-channel Attacks
First Poster Session

Noise-Free Security Assessment of Eviction Set Construction Algorithms with Randomized Caches
An open CAD flow to optimised key gate insertion in logic locking
Insertion of random delay with context-aware dummy instructions generator in a RISC-V processor
Second Poster Session
Thank you for your attention