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Verification of the CVA6 Open Source Core

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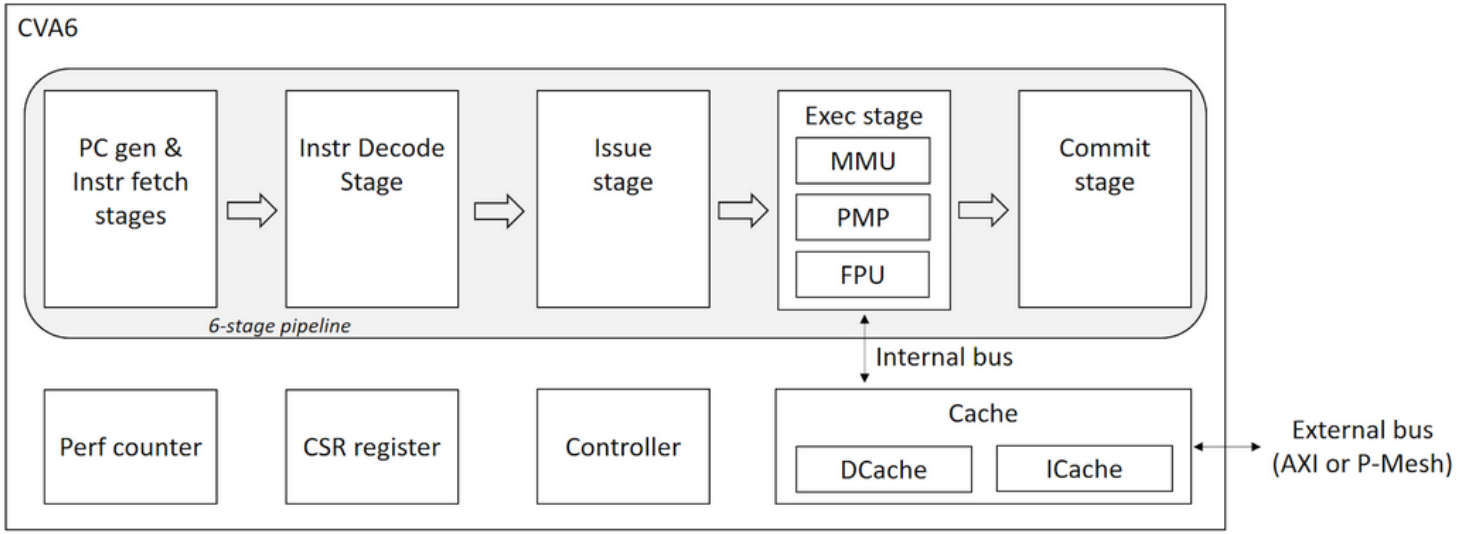
in collaboration with Thales TRT and ECC

CVA6 is a RISC-V implementation

- Designed by ETH Zürich
- Open Source, maintained by OPENHW GROUP PROVEN PROCESSOR IP
- Application processor, System Verilog



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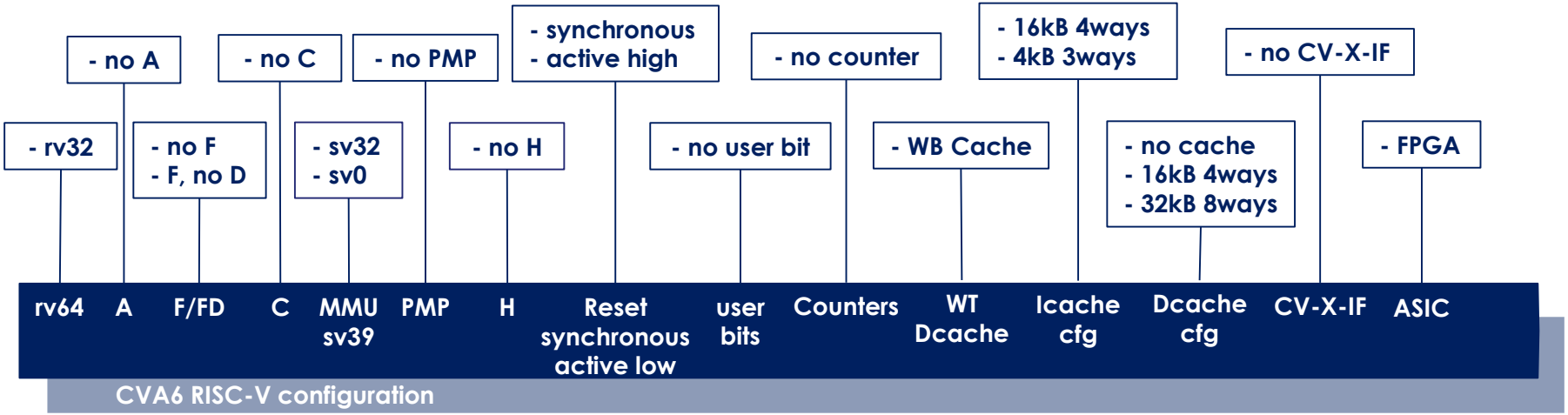
Verification challenges

Multi configuration

- Today CVA6 maturity is TRL3-4
- Many features and configurations



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Verification, what for?

CVA6 is a good climber but…

- Many features
- Multi configurations
  - Big: 500 kgates
  - Small: 80 kgates
- Multi targets
  - FPGA
  - ASIC

… cannot be industrialized as it is

- Functional bugs
  - Compromise product industrialization
  - Create security vulnerabilities and safety issues

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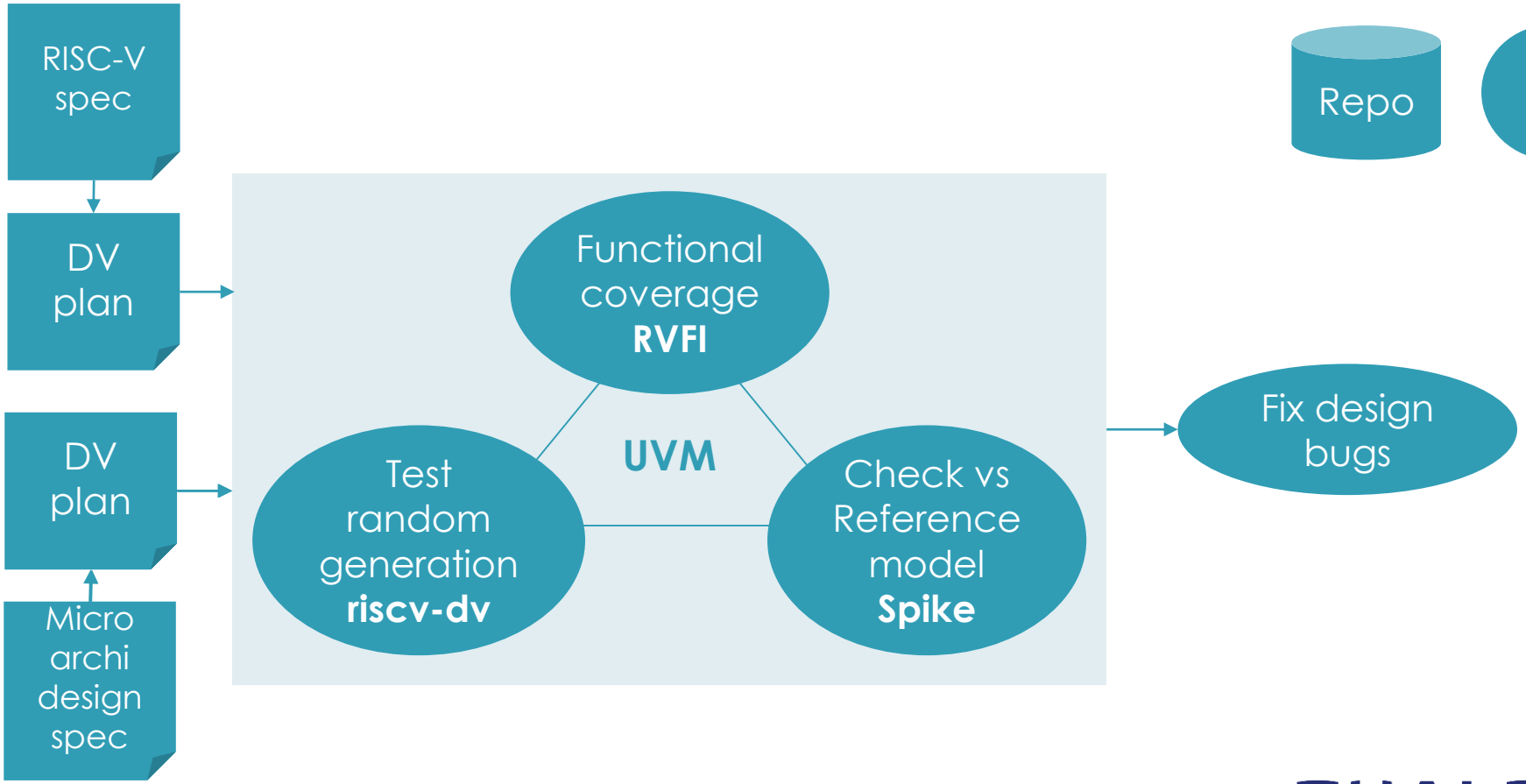
Verification methodology



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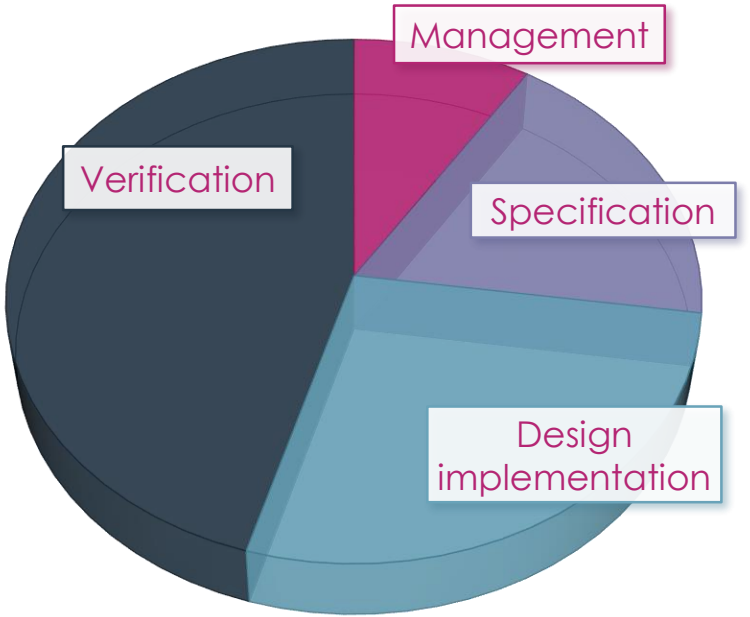
Verification cost

Verification more costly than design implementation!



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RISC-V to reuse verification

All RISC-V processors follow the same Instruction Set Architecture

- Unprivileged ISA, Privilege Architecture, External Debug Support

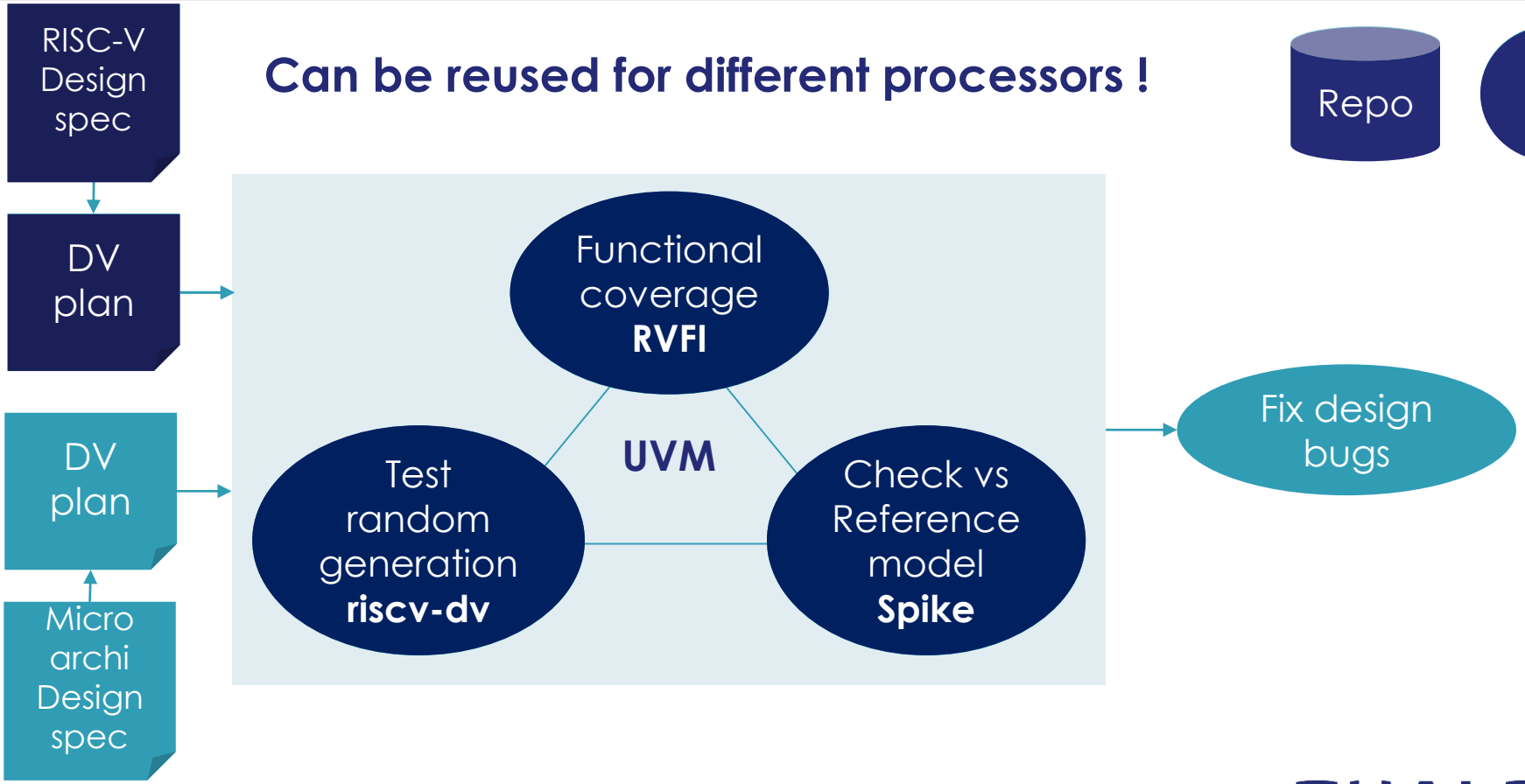
Related Design Verification Plans are identical

Verification methodology can be re-used by using same:

- Verification repository, e.g. OpenHW Group
- Reference model, e.g. Spike
- Random test generation, e.g. riscv-dv
- UVM agents
- Test regression suites, e.g. riscv-arch-test

Verification re-use

Can be reused for different processors !



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Collaborations

Thales is the main CVA6 industrial contributor

- OpenHW Group member
- Contributions in Design, Verification and OS support
- Committer in OpenHW Group GitHub repositories

But…

- Sharing a same verification framework makes sense
- If an organization plans to improve the maturity of a RISC-V processor (could be different from CVA6), collaboration is welcome!

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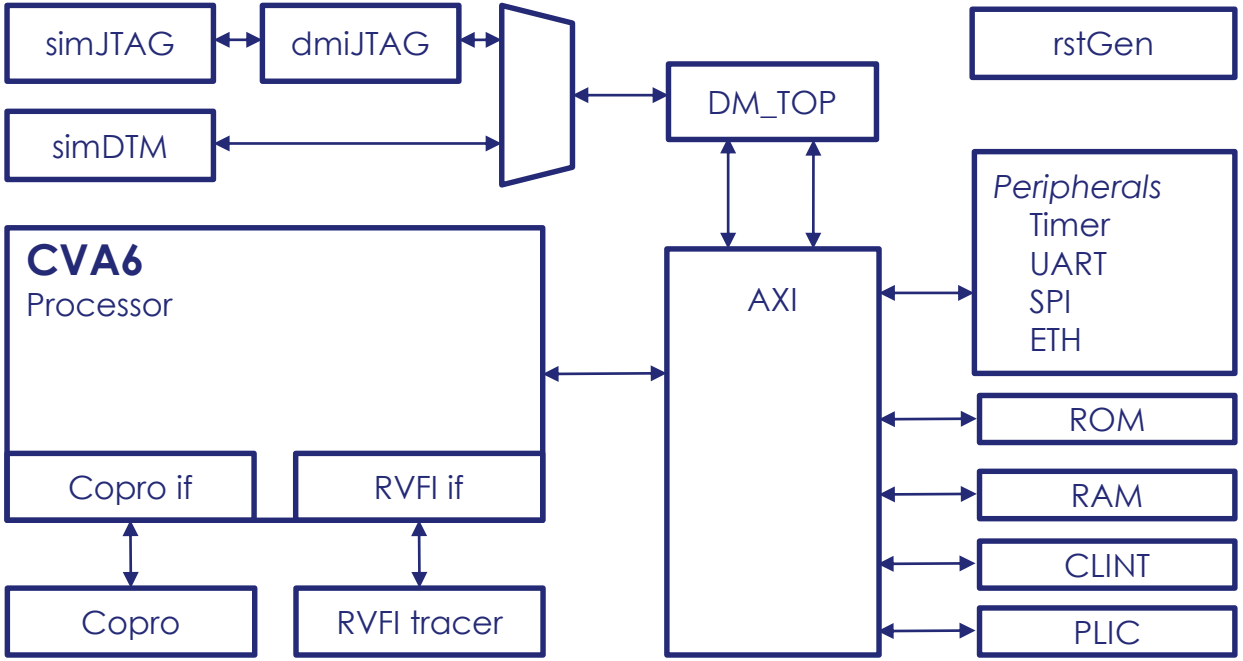
Verification infrastructure

First test bench - Testharness

Support digital simulation in platform environment



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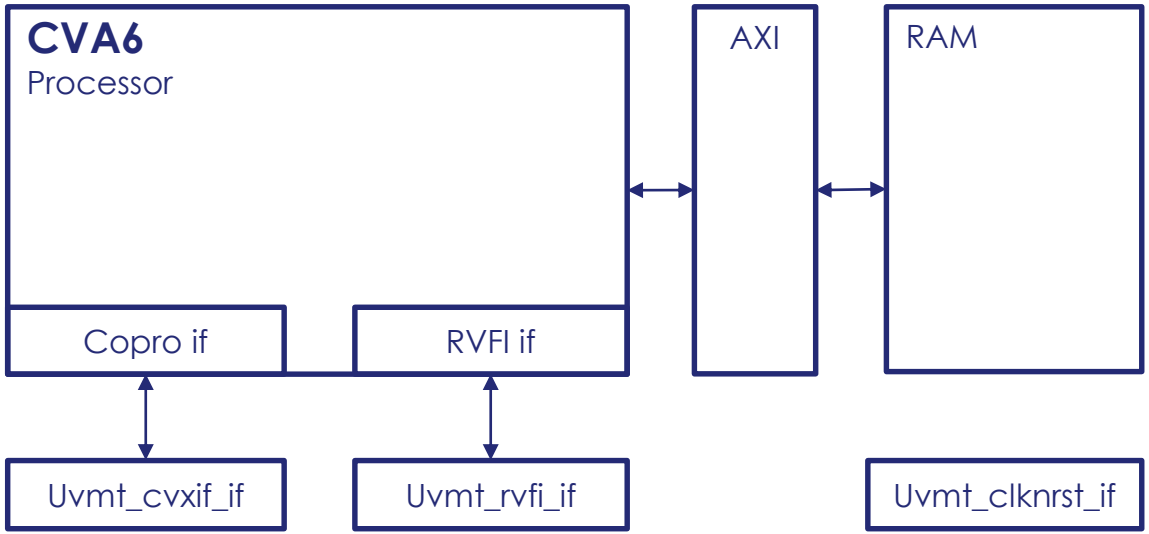
Second test bench - UVM

Support UVM verification environment



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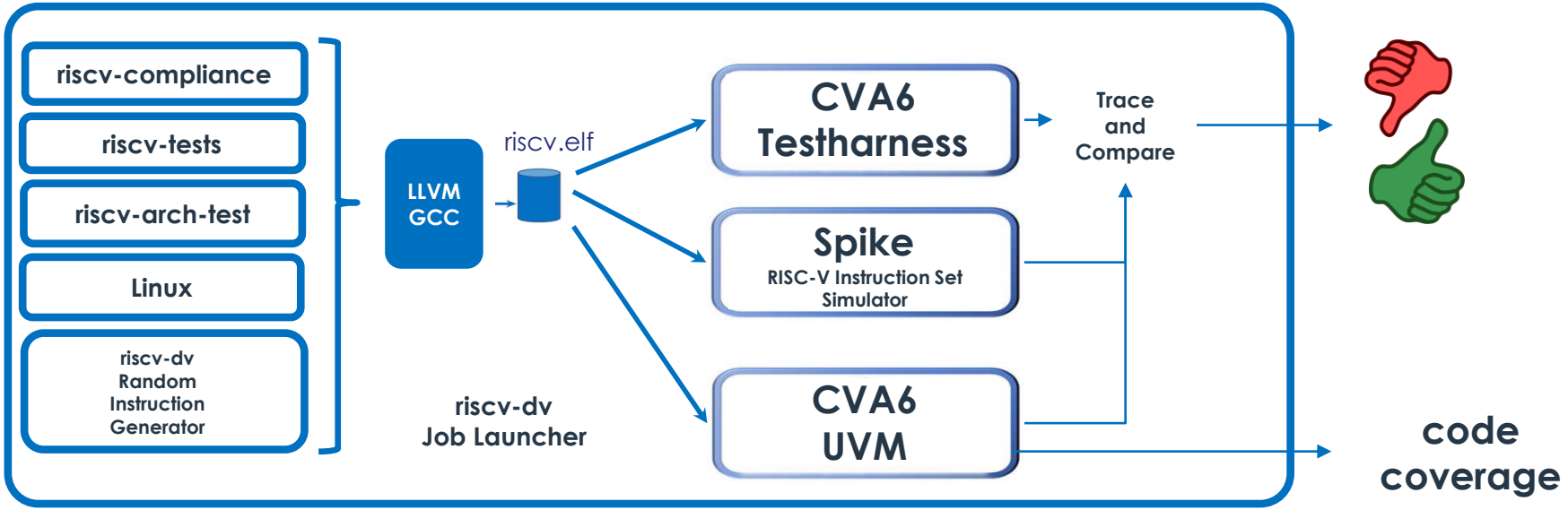
Verification flow



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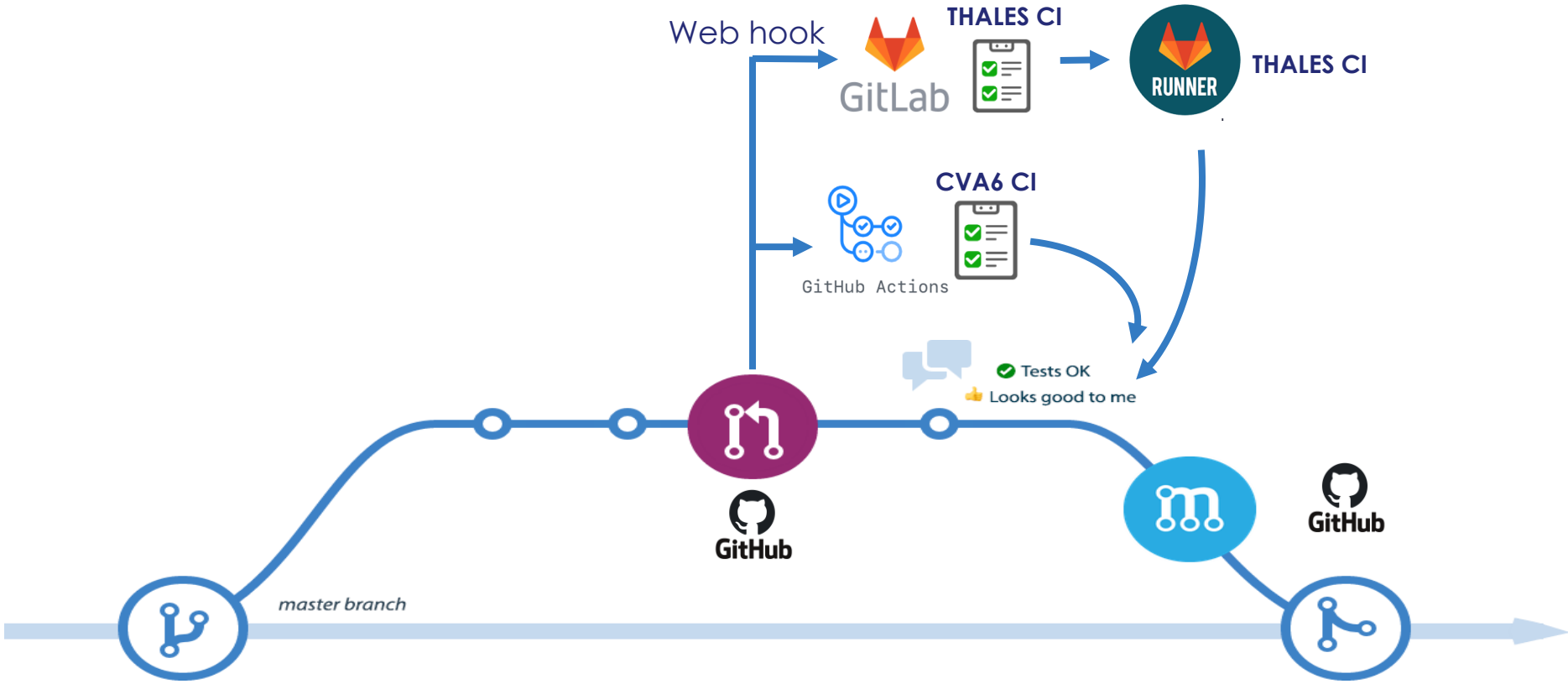
Pull Request workflow



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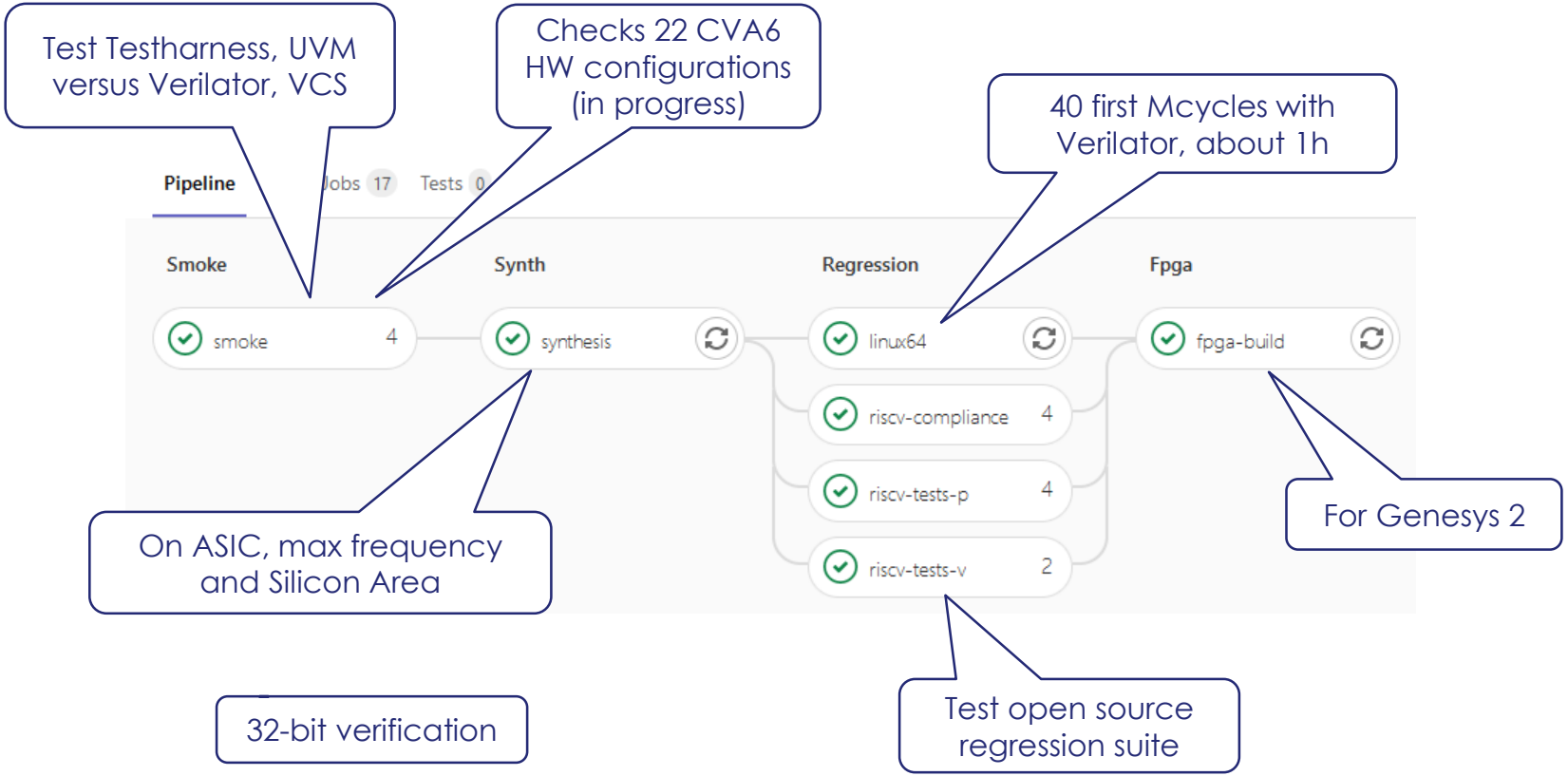
Continuous Integration checks



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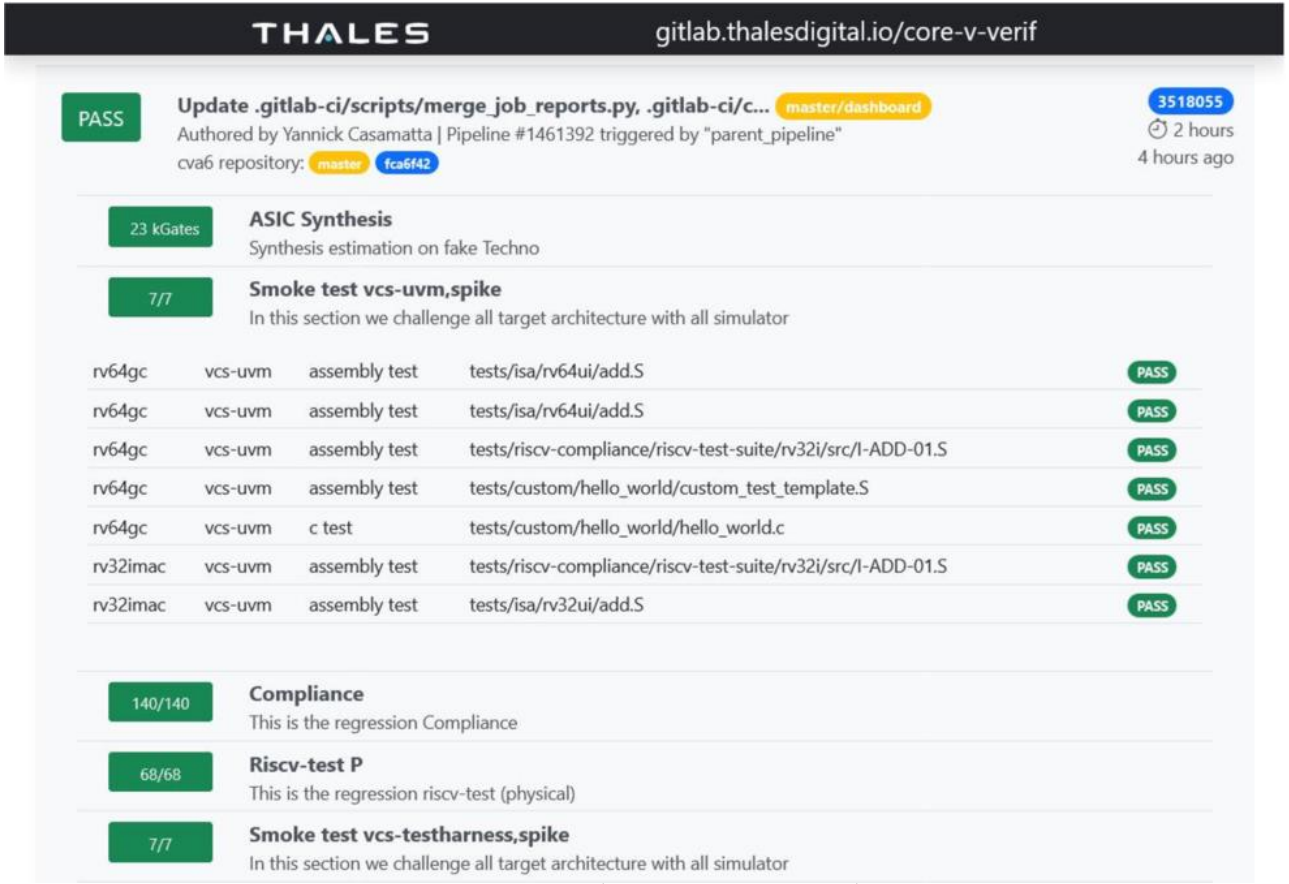
Dashboard



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Third test bench – FPGA

- Support Linux 64 and 32 bits execution
- Connect FPGA to run Linux boot during CI (in progress)

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Both RTL and verification are Open Source

Repositories

CVA6 requirement specification

- https://github.com/openhwgroup/cva6/blob/master/docs/specifications/cva6_requirement_specification.rst

CVA6

- RTL, testharness test bench and FPGA generation scripts
- https://github.com/openhwgroup/cva6

core-v-verif

- UVM test bench, random test generation, continuous integration
- https://github.com/openhwgroup/core-v-verif

CVA6 for Security Certification

Security Certification requests

- Right description of the test
  - functionalities / level of the test and test coverage
- Tests results
- At high level, certification body shall replay itself the test

Quality certification requests to monitor continuously results

CVA6 open source repository and continuous integration

- RTL and test codes
- Verification infrastructure to produce the test coverage

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THANK YOU!

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