

Verification of the CVA6 Open Source Core

2022-05-04

Jean-Roch COULON - Thales DIS (INVIA)
in collaboration with Thales TRT and ECC

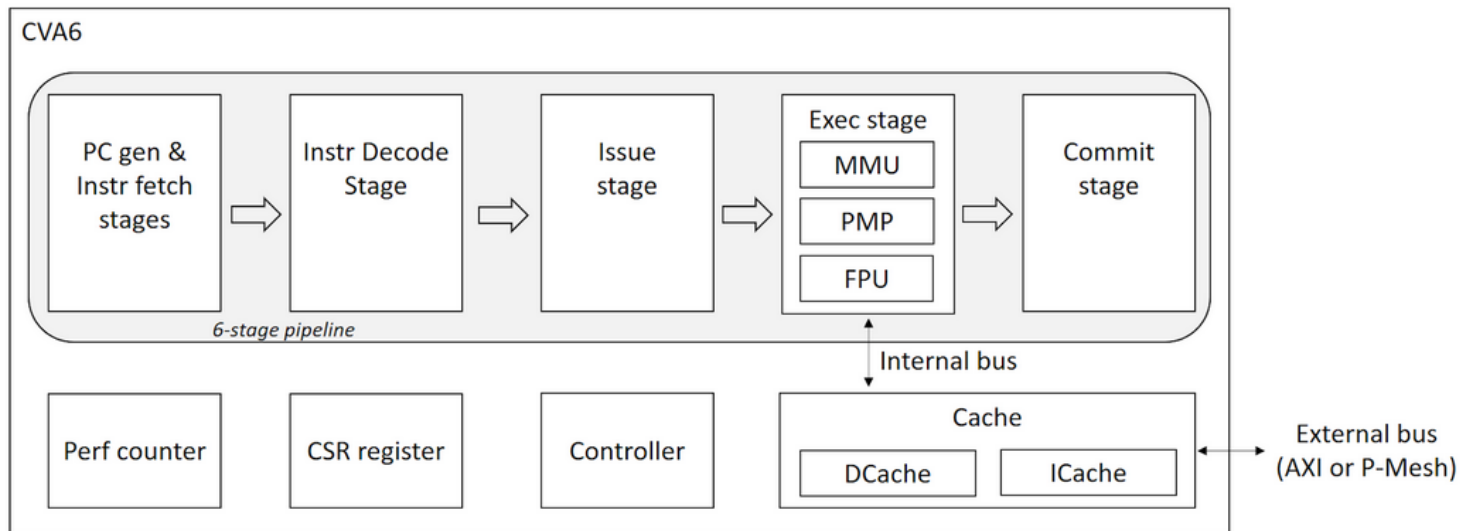


CVA6 is a RISC-V implementation

Designed by ETH Zürich

Open Source, maintained by  **OPENHW** GROUP™
PROVEN PROCESSOR IP

Application processor, System Verilog



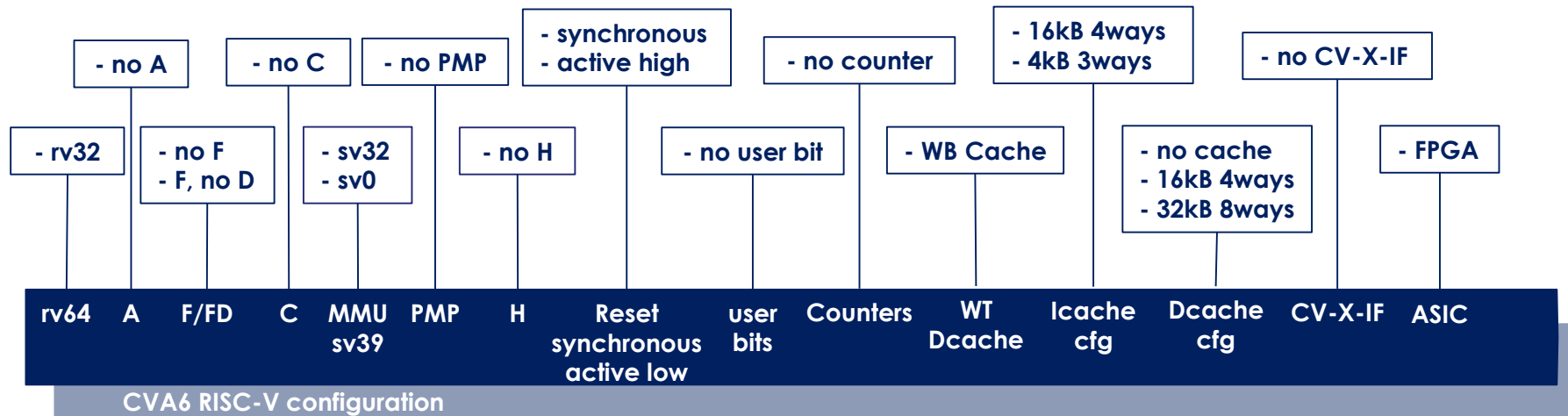
THALES

Verification challenges



Today CVA6 maturity is TRL3-4

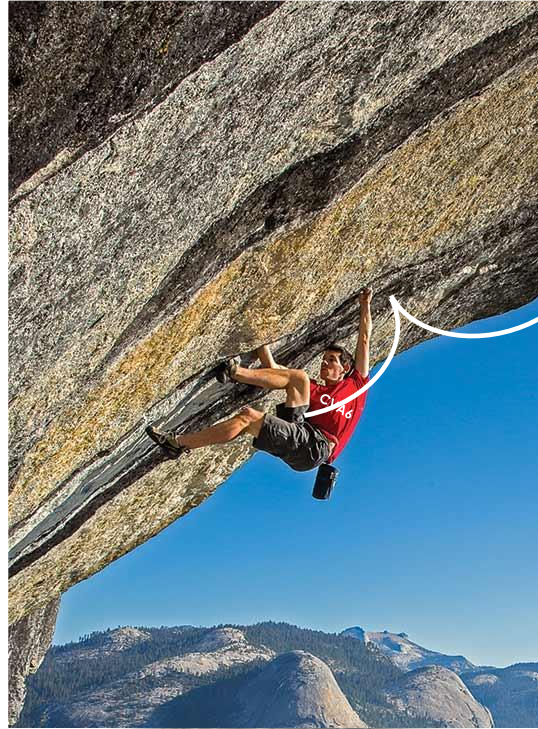
Many features and configurations



Verification, what for?

CVA6 is a good climber but...

- Many features
- Multi configurations
 - Big: 500 kgates
 - Small: 80 kgates
- Multi targets
 - FPGA
 - ASIC

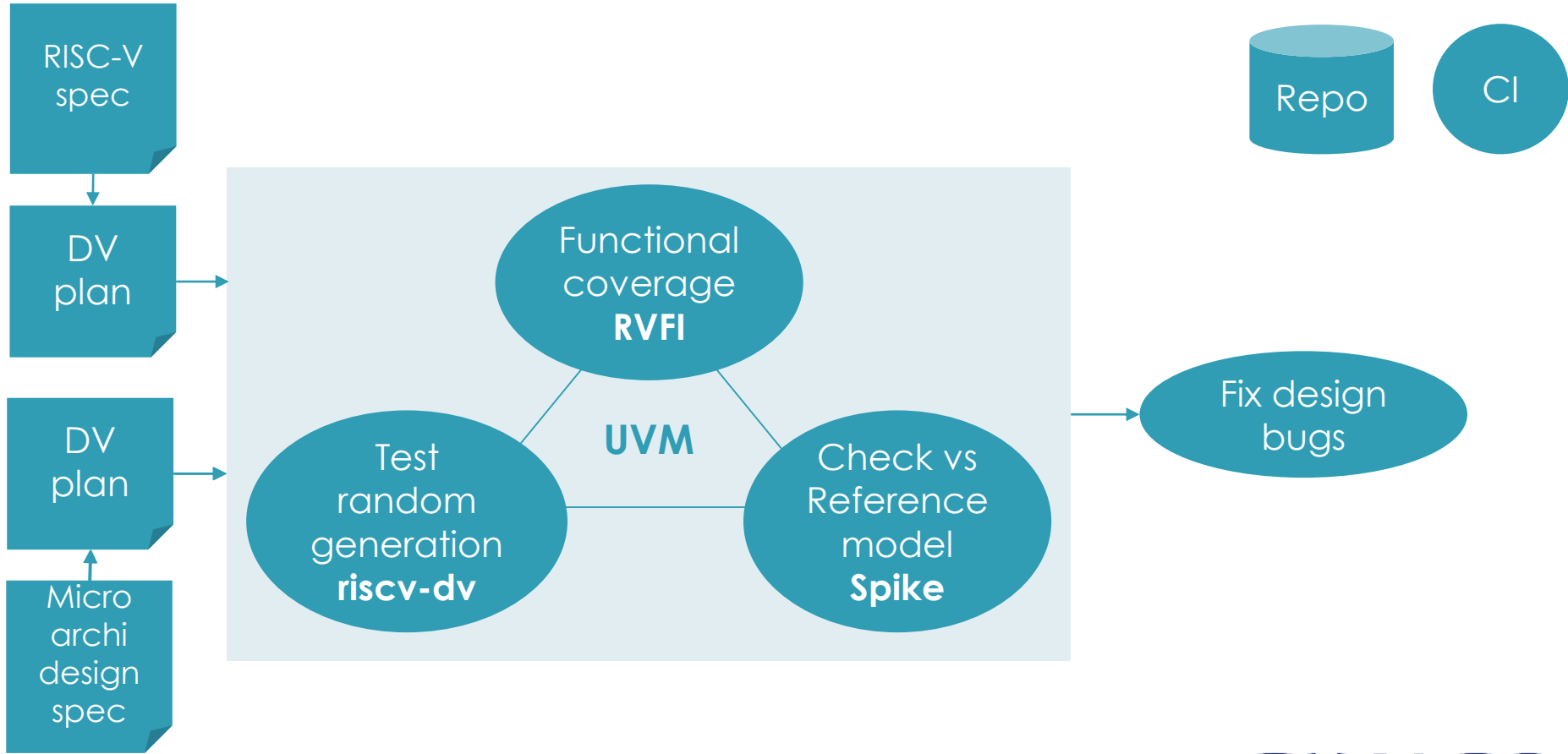


... cannot be industrialized as it is

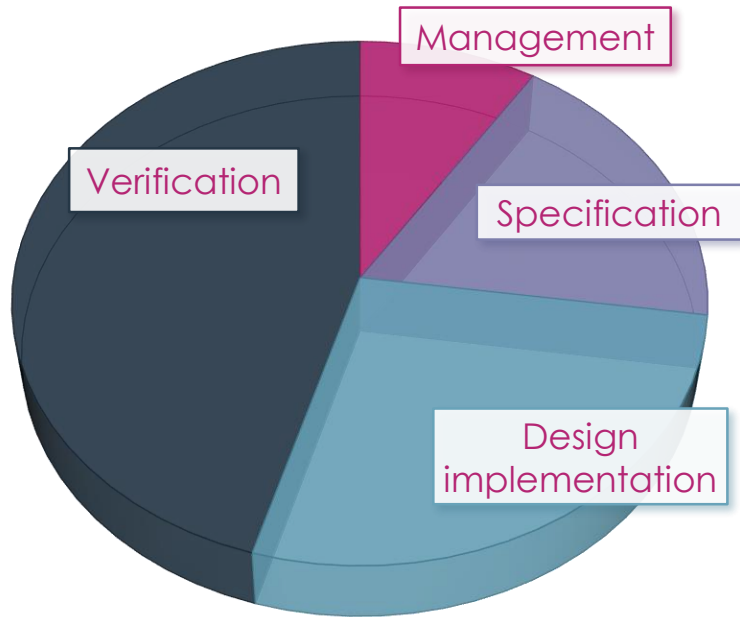
- Functional bugs
 - Compromise product industrialization
 - Create security vulnerabilities and safety issues



Verification methodology



Verification more costly than design implementation!



RISC-V to reuse verification

■ All RISC-V processors follow the same Instruction Set Architecture

- Unprivileged ISA, Privilege Architecture, External Debug Support

■ Related Design Verification Plans are identical

■ Verification methodology can be re-used by using same:

- Verification repository, e.g. OpenHW Group
- Reference model, e.g. Spike
- Random test generation, e.g. riscv-dv
- UVM agents
- Test regression suites, e.g. riscv-arch-test

Can be reused for different processors !

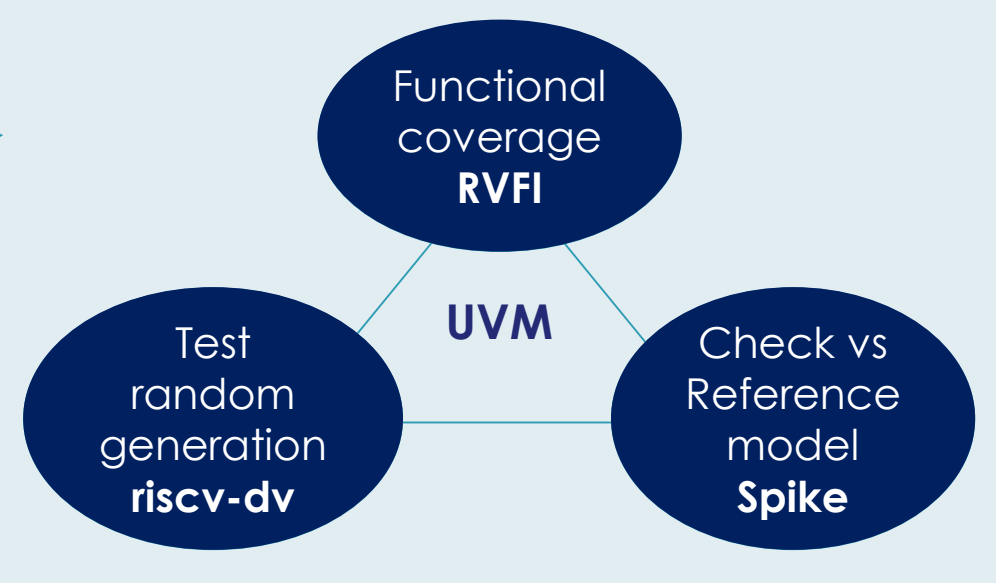


RISC-V
Design
spec

DV
plan

DV
plan

Micro
archi
Design
spec



Fix design
bugs

Thales is the main CVA6 industrial contributor

- OpenHW Group member
- Contributions in Design, Verification and OS support
- Committer in OpenHW Group GitHub repositories

But...

- Sharing a same verification framework makes sense
- If an organization plans to improve the maturity of a RISC-V processor (could be different from CVA6), collaboration is welcome!

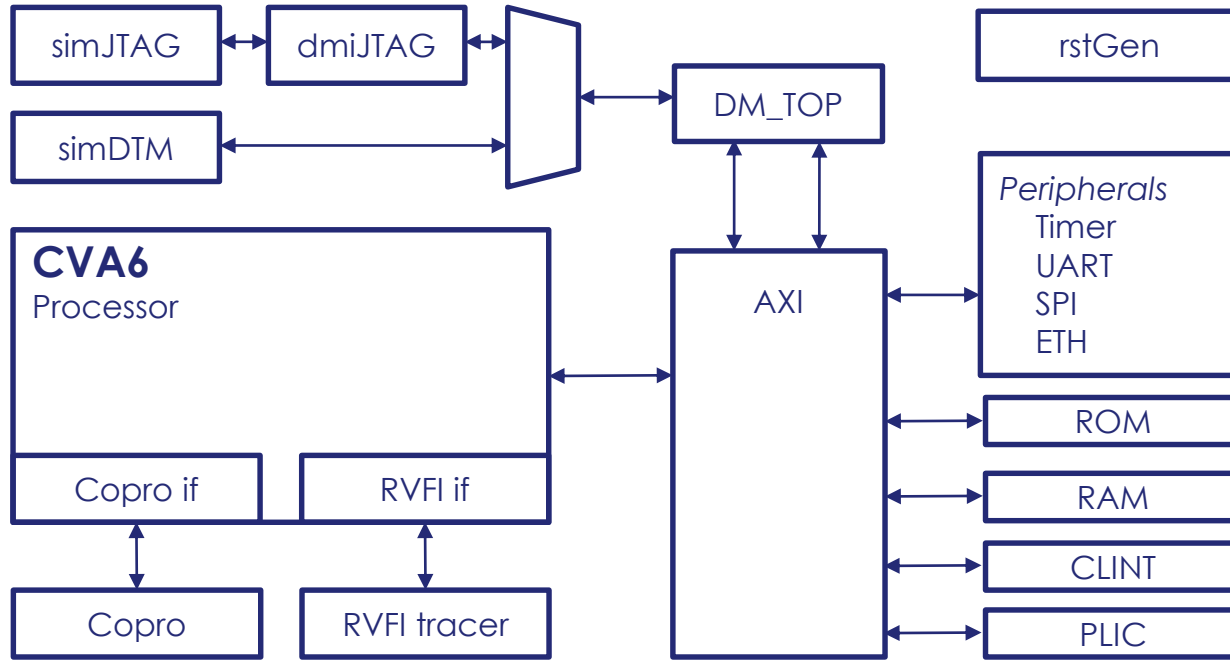
THALES

Verification infrastructure

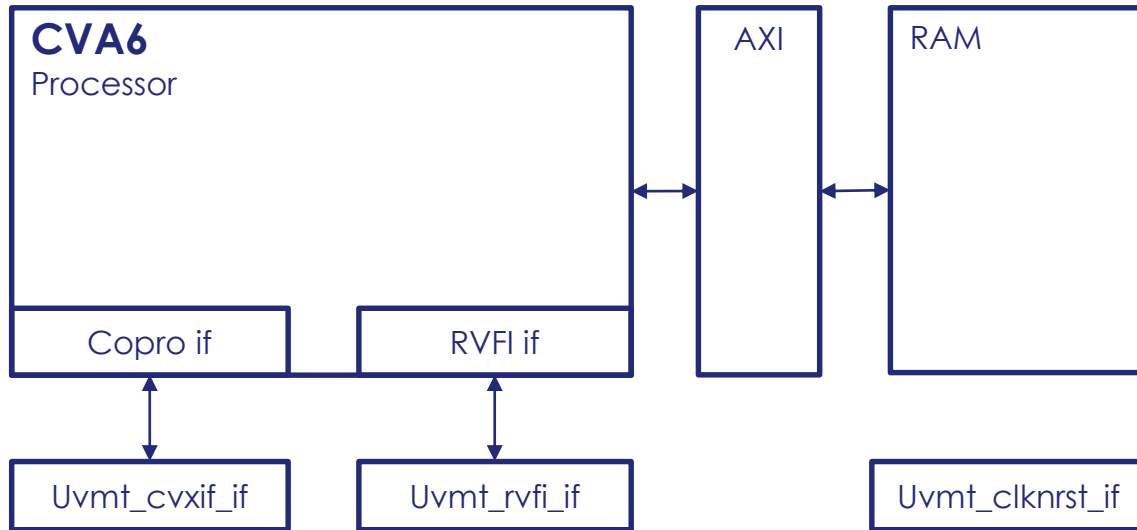


First test bench - Testharness

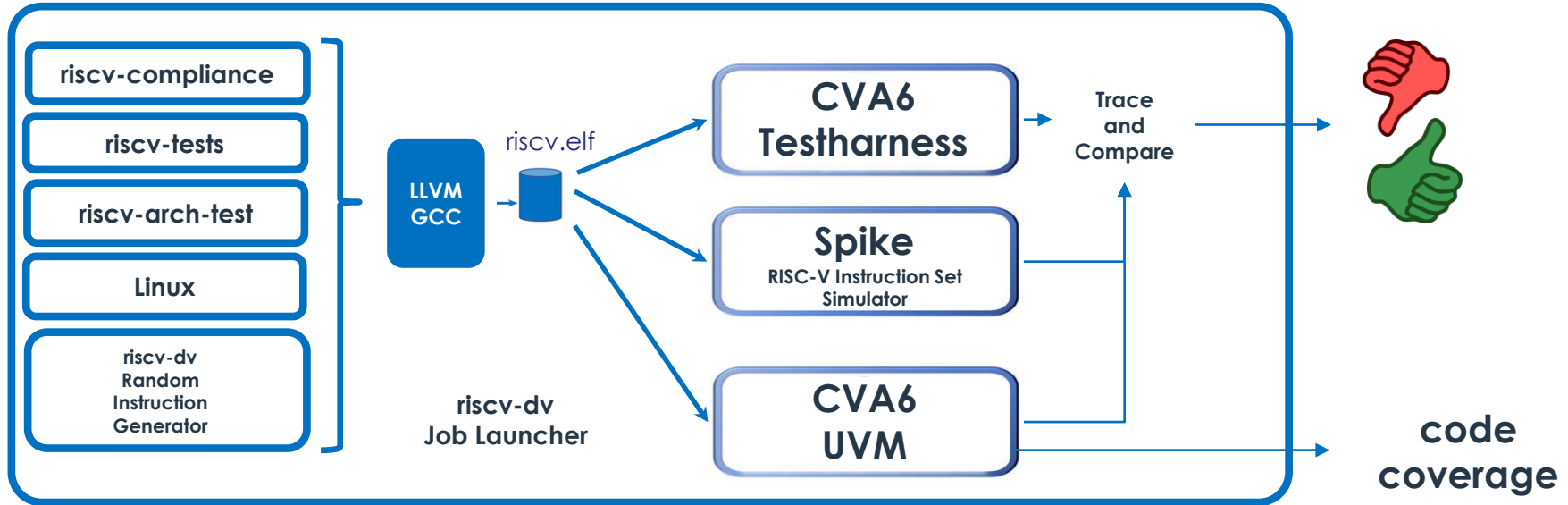
Support digital simulation in platform environment



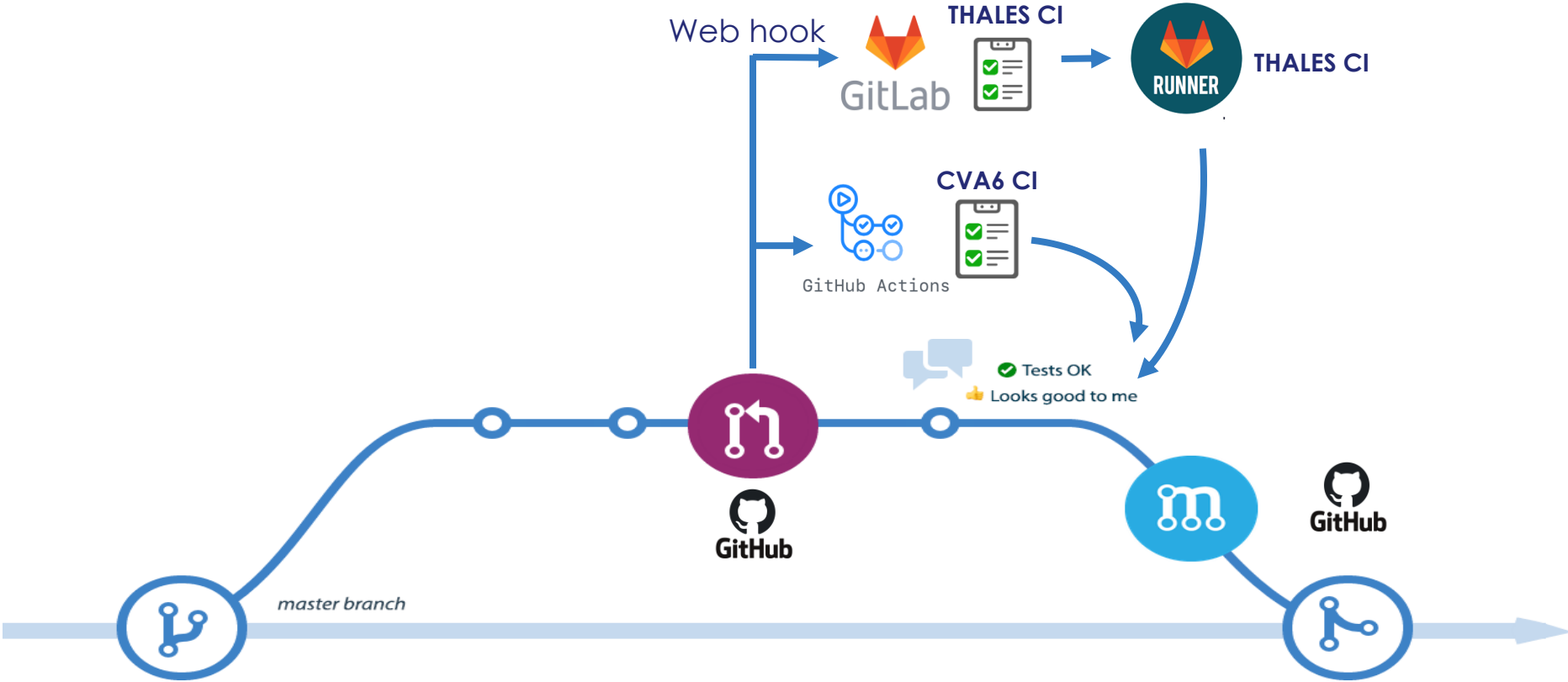
Support UVM verification environment



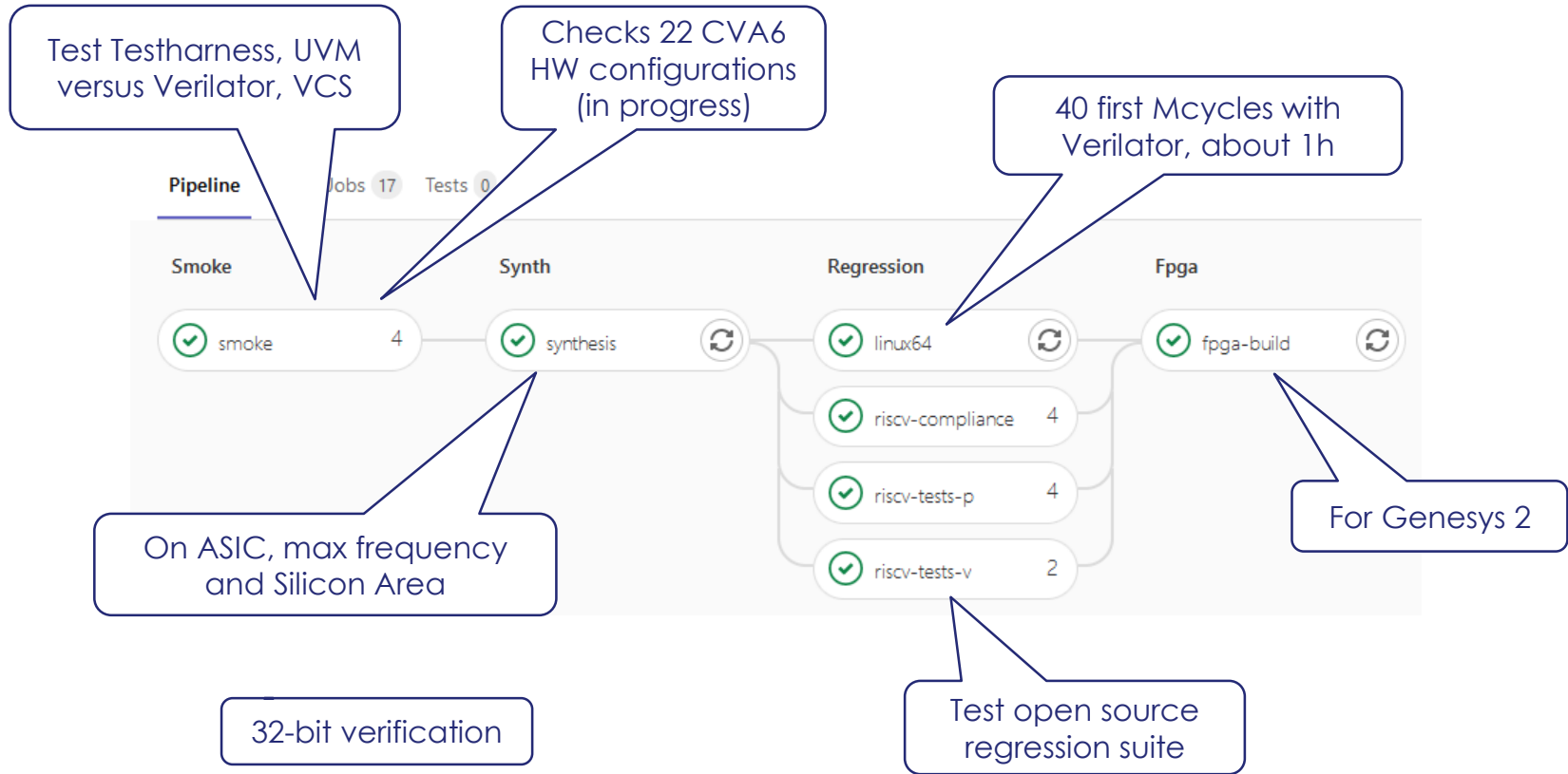
Verification flow



Pull Request workflow



Continuous Integration checks



PASS

Update .gitlab-ci/scripts/merge_job_reports.py, .gitlab-ci/c... master/dashboard

Authored by Yannick Casamatta | Pipeline #1461392 triggered by "parent_pipeline"

cva6 repository: master fca6f42

3518055

🕒 2 hours
4 hours ago

23 kGates

ASIC Synthesis

Synthesis estimation on fake Techno

7/7

Smoke test vcs-uvm,spike

In this section we challenge all target architecture with all simulator

rv64gc	vcs-uvm	assembly test	tests/isa/rv64ui/add.S	PASS
rv64gc	vcs-uvm	assembly test	tests/isa/rv64ui/add.S	PASS
rv64gc	vcs-uvm	assembly test	tests/riscv-compliance/riscv-test-suite/rv32i/src/l-ADD-01.S	PASS
rv64gc	vcs-uvm	assembly test	tests/custom/hello_world/custom_test_template.S	PASS
rv64gc	vcs-uvm	c test	tests/custom/hello_world/hello_world.c	PASS
rv32imac	vcs-uvm	assembly test	tests/riscv-compliance/riscv-test-suite/rv32i/src/l-ADD-01.S	PASS
rv32imac	vcs-uvm	assembly test	tests/isa/rv32ui/add.S	PASS

140/140

Compliance

This is the regression Compliance

68/68

Riscv-test P

This is the regression riscv-test (physical)

7/7

Smoke test vcs-testharness,spike

In this section we challenge all target architecture with all simulator

Third test bench – FPGA

- Support Linux 64 and 32 bits execution
- Connect FPGA to run Linux boot during CI (in progress)



THALES

Both RTL and verification are Open Source





CVA6 requirement specification

- https://github.com/openhwgroup/cva6/blob/master/docs/specifications/cva6_requirement_specification.rst

CVA6

- RTL, testharness test bench and FPGA generation scripts
- <https://github.com/openhwgroup/cva6>

core-v-verif

- UVM test bench, random test generation, continuous integration
- <https://github.com/openhwgroup/core-v-verif>

Security Certification requests

- Right description of the test
 - functionalities / level of the test and test coverage
- Tests results
- At high level, certification body shall replay itself the test



Quality certification requests to monitor continuously results

CVA6 open source repository and continuous integration

- RTL and test codes
- Verification infrastructure to produce the test coverage

THALES



THANK YOU!

Thales DIS (INVIA)

www.thalesgroup.com

