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French RISC-V Student Contest: Lessons Learned

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Why a RISC-V student contest in France ?

- Encourage students working on hardware processor architecture
- Promote RISC-V technologies in academic laboratories
- Expand RISC-V and OpenHW communities in France
- Strengthen RISC-V cooperation between academics and the industry

For French universities (Master level, ≈MSEE)

Jointly organized by

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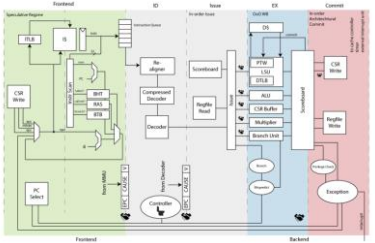
Target the Thales promoted RISC-V processor CVA6



OPENHW GROUP
PROVEN PROCESSOR IP

Optimize the performance of the CVA6 FPGA implementation

Timeline

- **Summer 2020: Assessing universities' interest**
- **2020-09-25: Kick off**
- **2020-10-18: Preliminary technical kit available**
  - Simulation, FPGA synthesis
- **2020-12-07: Complete technical kit available**
  - Adding FPGA board support
- **2021-04-23: Result submission**
- **2021-06-03: Oral defense**
- **2021-06-09: Prize ceremony**
- **June 2021: Surveying feedback from participants**

The results

13 teams from 10 universities, 2-4 students per team, 5 results submitted

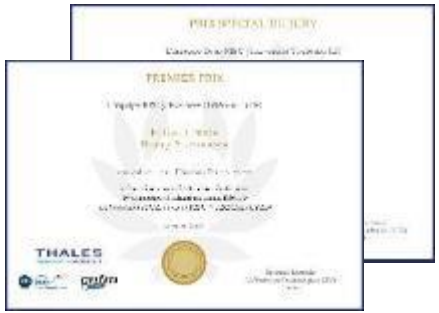
1st

RISCy Business (Télécom Paris)
Optimizations targeting FPGA technology
+22% frequency, -6% resource usage
5000 €

2nd

Agence Tous RISC (Toulouse III)
Added one ALU (the superscalar way)
+19% CoreMark/MHz, +37% resource usage
2000 €

Ceremony at GDR SOC² annual event:
68 attendees on site (+ online)
Awards handed by Thales software VP

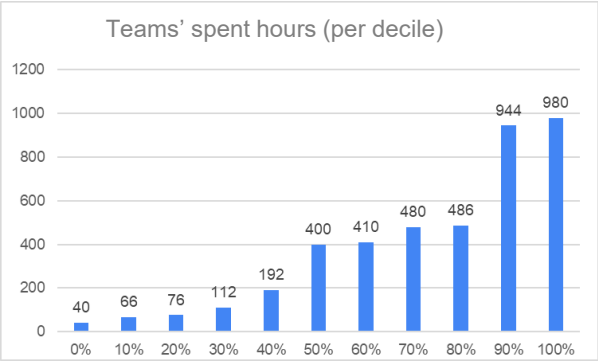


Feedback from participants

Project type:

- 3 teams: free-time project
- 8 teams: curriculum project

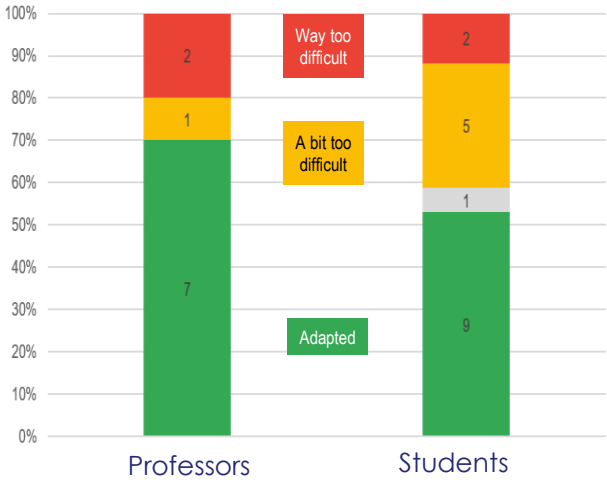
Strong team involvement



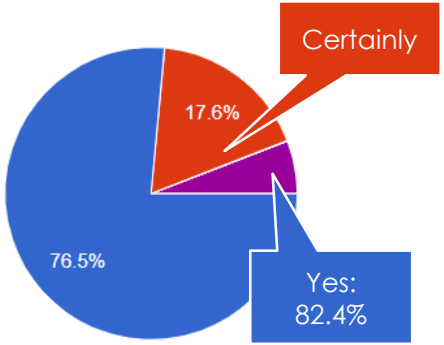
Team's effort as estimated by each respondent.

Common difficulties

- COVID: remote teams, motivation
- Provisioning EDA licenses
- Setting up the IT (servers, VMs, Linux…)
- Many tools to harness
- Technical complexity

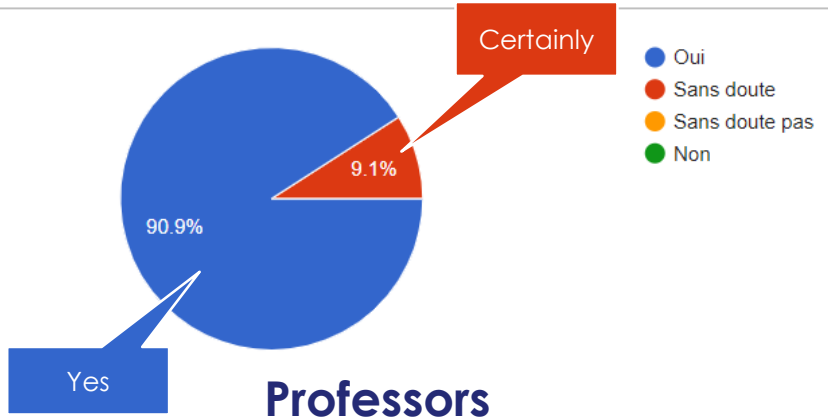


Do it again ?



Students

- Oui
- Sans doute
- Sans doute pas
- Non
- Oui : dans les faits nous avons eu beaucoup de mal à avancer en étant séparés, et nous avons surtout progressé lorsqu'on arrivait à travailler ensemble physiquement



Professors

How to improve ?

- Pre-installed/configured dev environment
- Fine tune technical complexity
- Internal & External communications
- Community Manager to maintain engagement
- Communication tools (switch to Discord)
- Intermediary meet-up with teams

2021-2022 edition

- Based on participants' feedback, launched new edition
- Same organization team
- Same HW base (CVA6 core, FPGA board)
- Objective: optimize CVA6 **energy efficiency** on the MNIST CNN algorithm

- 12 teams from 7 universities have applied
- Calendar:
  - Kickoff: 2021-11-02
  - Result submission: 2022-04-22 (extension to 2022-05-23)

Extending the contest to other geographies?

Set up organization team

- Significant organization effort
- Main activities:
  - Technical (set up, verify and maintain kits, support teams, review teams' results)
  - External communication (promote contest in universities)
  - Internal communication (run forums, lead internal events)
  - Assist teams in provisioning (EDA vendors' university programs, FPGA dev board brokerage)

Open-source repo as a starting point

- Source code, rules and guidance: https://github.com/thalesgroup/cva6-softcore-contest
- 2021-2022 contest online
- 2020-2021 edition available through a tag
- Only a few non-blocking tips and tricks have infused on the closed Discord forum

Impact on academic communities

Very positive feedback during the prize ceremony

Close to CVA6:

- RISC-V and CVA6 adopted in a few master curricula in France
- One 2020-2021 student has started a PhD thesis with CVA6
- 2 ANR national research projects awarded

… and those we don't know…

More generally

- GDR SOC² gathers an increasing number of scientific presentations on RISC-V and open-source hardware.

But

- Very few French universities and research centers involved in RISC-V International and open-source alliances

Getting in touch

The contest organizers:

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Discussion