Vitruvius+: An Area-Efficient RISC-V Decoupled Vector Accelerator for High Performance Computing

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Introduction
Vitruvius+ is a key component of the European Processor Initiative (EPI), a project co-funded by the European Union.

Aims to design and implement a roadmap for a new family of low-power Exascale European processors.

First phase concluded with a test-chip taped out in June 2021 using GLOBALFOUNDRIES 22FDX® 22nm FD-SOI running at 1 GHz.

Vitruvius+ is part of the first tapeout in the second phase of EPI.

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Microarchitecture
Why Vitruvius+

- Vitruvius+ is an improved version of Vitruvius, the vector execution core of the first phase of EPI, presented at the RISC-V Summit 2021 [1]
- Vitruvius+ inherits all the main characteristics of Vitruvius:
  - Implements version 0.7.1 of the RISC-V vector extension (RVV)
  - Long vectors, up to 256 DP-elements
  - Increases vector length up to 2048 DP-elements when grouping 8 vectors (LMUL=8)
  - Support mixed width vector operations, namely widening and narrowing
  - Decoupled architecture
  - Lightweight out-of-order execution
  - Vector register renaming
  - Vector instructions overlapping
  - Multiple accumulators enhancing reduction operations

Vitruvius+ New Features

- Vector memory-to-arithmetic instruction chaining
- Tree-based reduction algorithm to further improve performance
- Enhanced memory units to manage more than one in-flight memory operations
  - Up to three vector strided loads and stores
  - Up to one masked/indexed memory instruction at a time
  - Two additional strided loads or stores can be handled while executing a masked/indexed memory operation
- Unidirectional ring inter-lane interconnect with limited reconfiguration
- Completely configurable design
  - Independent vector lanes
  - Variable vector length
  - Parameterized functional unit pipeline depths
Execution Paradigm

- Vitruvius+ adopts a **hybrid in-order/out-of-order** execution scheme
  - Arithmetic instructions proceed in-order
  - Memory instructions can execute out-of-order
- Vitruvius+ is a **decoupled accelerator**
  - Offload vector instructions from the scalar pipeline
  - Only vector memory instructions need the scalar core and the vector accelerator to effectively interact
- Communication with the scalar core is possible through the **Open Vector Interface (OVI)**

An overview of the OVI, the interface resulting from the joint effort between Semidynamics and the BSC (https://github.com/semidynamics/OpenVectorInterface).
Vitruvius Block Diagram
Lane Architecture

- 8 vector lanes in the baseline configuration, connected through an area-efficient ring interconnect
- A local FSM orchestrates intra-lane data movements
- A control unit selects the active/inactive elements
- Separated mask registers from the register file to avoid read conflicts on predicated instructions
- One ALU for all integer and logical operations
- One FPU for floating-point operations
- Dedicated vector reduction logic
Vector Register File Organization

- Interleaved vector registers across the lanes, each one holding 5 SRAM banks
- Each SRAM bank is 2 KB:
  - Accounts for 10 KB of SRAM per lane
  - Instantiates 80 KB for the vector register file (VRF) in the 8 lane configuration
  - Allocates space for the 32 architectural registers and 8 additional renaming registers
  - Each register holds a maximum of 256 64-bit elements
- Vector registers are contiguously stored in the banks
- A read always tries to get a full row from the banks
- A write can store whatever number of elements

<table>
<thead>
<tr>
<th>LANE</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>B4</td>
<td>0</td>
<td>1</td>
<td>6</td>
<td>8</td>
<td>9</td>
<td>0</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>B3</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>B2</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>7</td>
<td>8</td>
</tr>
<tr>
<td>B1</td>
<td>8</td>
<td>9</td>
<td>0</td>
<td>1</td>
<td>2</td>
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<td>4</td>
<td>5</td>
</tr>
<tr>
<td>B0</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>0</td>
</tr>
</tbody>
</table>

- A read always tries to get a full row from the banks
- A write can store whatever number of elements

![Table of Vector Register File Organization](image-url)
Inter-lane Interconnect
Inter-lane Interconnect

Node i

From Node \( n \text{ Lanes} \times \text{node} \)

From Node \( (n+1) \text{ Lanes} \times \text{node} \)

DIR

inject

eject

WE

CLK

64

64
Reductions Enhancement

- Vitruvius+ introduces an additional optimization on the execution of vector reductions
- Apart from implementing multiple accumulators for the intra-lane reduction phase, it proceeds through inter-lane tree-based algorithm to parallelize arithmetic operations
Evaluation
Vitruvius+ was synthesized for GLOBALFOUNDRIES 22FDX® 22nm FD-SOI
Target frequency for the standalone synthesis was 1.4 GHz

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
<td>Value</td>
</tr>
<tr>
<td>Number of lanes</td>
<td>8</td>
</tr>
<tr>
<td>VRF size</td>
<td>10 KiB/lane</td>
</tr>
<tr>
<td>Number of banks</td>
<td>5 banks/lane</td>
</tr>
<tr>
<td>Bank width</td>
<td>64 bits</td>
</tr>
<tr>
<td>Number of ports</td>
<td>1 port/bank</td>
</tr>
<tr>
<td>Number of slots</td>
<td>256 slots/bank</td>
</tr>
</tbody>
</table>

Results reported for a synthesis run using typical conditions (TT, 0.80 V, 25 °C)
Physical Design

Area breakdown for the single lane. The FPU occupies most of it.

Layout resulting from the place-and-route of an instance of Vitruvius+ with 8 lanes.
### Vectorized Benchmarks

- Several vectorized benchmarks were used to characterize Vitruvius+
- We used problem sizes that are beneficial for our vector unit

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>DP-FLOP/cycle</th>
<th>DP-GFLOPS (@1,4GHz)</th>
<th>Speed-Up on Vitruvius</th>
</tr>
</thead>
<tbody>
<tr>
<td>Matmul 256x256</td>
<td>15.5</td>
<td>21.7</td>
<td>1.02X</td>
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<tr>
<td>Jacobi-2D</td>
<td>8.2</td>
<td>11.5</td>
<td>1.1X</td>
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<td>Black-Scholes</td>
<td>6</td>
<td>8.4</td>
<td>1.17X</td>
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<td>LavaMD</td>
<td>6.6</td>
<td>9.24</td>
<td>1.12X</td>
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<td>Pathfinder</td>
<td>3.0</td>
<td>4.2</td>
<td>1.16X</td>
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<tr>
<td>Streamcluster</td>
<td>7.1</td>
<td>9.94</td>
<td>1.8X</td>
</tr>
</tbody>
</table>
Future Plan
Vitruvius+ successor

- EVA (Enhanced Vitruvius Architecture), Vitruvius+ successor, is the vector accelerator of the second phase of EPI

- EVA will be designed with the following features in mind:
  - Implements the RISC-V V-extension release 1.0
  - New scalar core interface (OVI 2.0) being ratified
  - Higher performance inter-lane interconnect
  - Higher clock frequency (2.0 GHz)
  - New fabrication technology (GF12LP) in the EPI project
  - Explore different VRF configurations
Towards RVV-1.0

- RVV-1.0 introduce novel features for the vector architecture specifications:
  - New mask layout. Simplified mask bits mapping to the vector register v0 (mask bit $n$ matches bit $n$ of v0)
  - Vector tail agnostic and mask agnostic. Dedicate bits vta and vma in the CSR vtype to control the behavior of tail elements and inactive masked-off elements, respectively
  - Fractional LMUL (LMUL<1). Reduces the number of bits used in a single vector register and increases the effective number of vector register groups when operating on mixed-width values
  - Memory operations variants. Allow different data and indices element sizes, include whole register loads/stores
Mask Layout Challenges

- The new mask layout, while simpler than in previous versions, is problematic for EVA
- There is the need of shuffling the mask bits among the lanes to deal with the mapping
Conclusion
Remarks

- Vitruvius and Vitruvius+ are the first of a family of vector accelerators developed at BSC.
- Vitruvius+ is the only RISC-V vector processor that supports long vectors (256 DP-elements per vector, up to 2048 DP-elements for the higher \textit{LMUL} configuration).
- Vitruvius+ is the first RISC-V vector processor compliant with the OVI specifications.
- EVA, Vitruvius+ successor, will fully support RVV-1.0 with the same maximum vector length, and will run at higher frequencies.
- This work shows that a long-vector accelerator can be designed following an area-efficient approach.
Acknowledgement

We express our gratitude to all the EPI partners
Thank you

Questions?

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