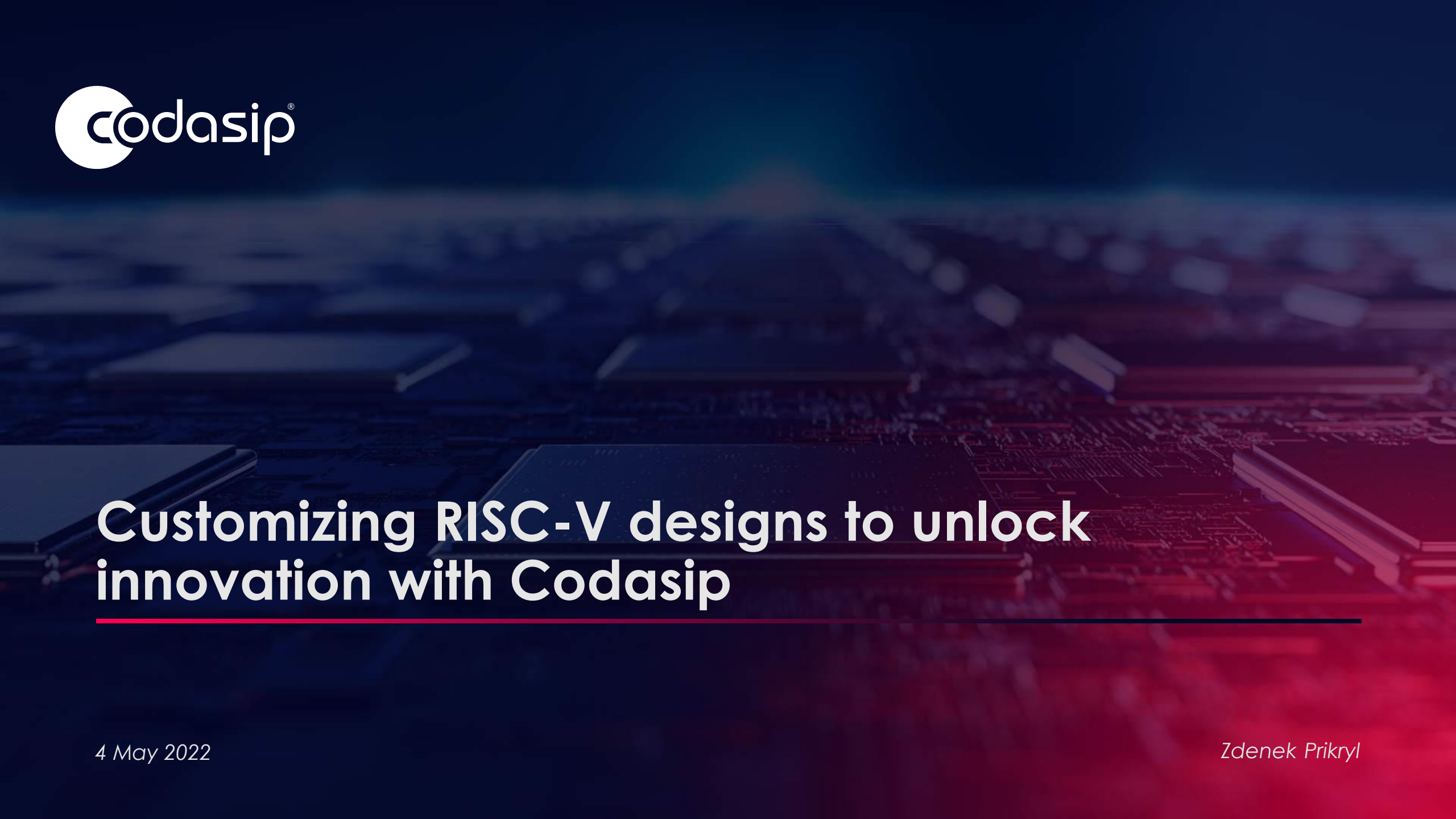


Customizing RISC-V designs to unlock innovation with Codasip

4 May 2022

Zdenek Prikryl

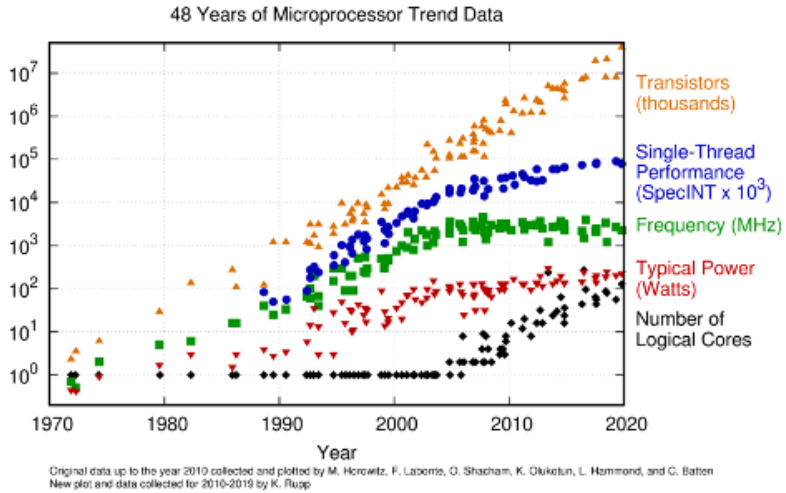
Codasip

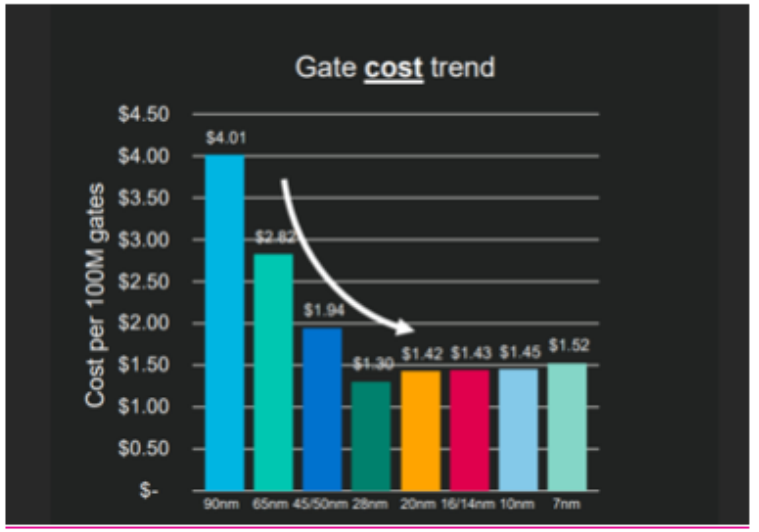
- Founded in 2014
- 140+ employees
  - More than 80% in R&D
- Released the 1st commercial RISC-V core
  - Now over 2 billion cores shipped

Based in Europe with offices all around the world

Scaling is Failing

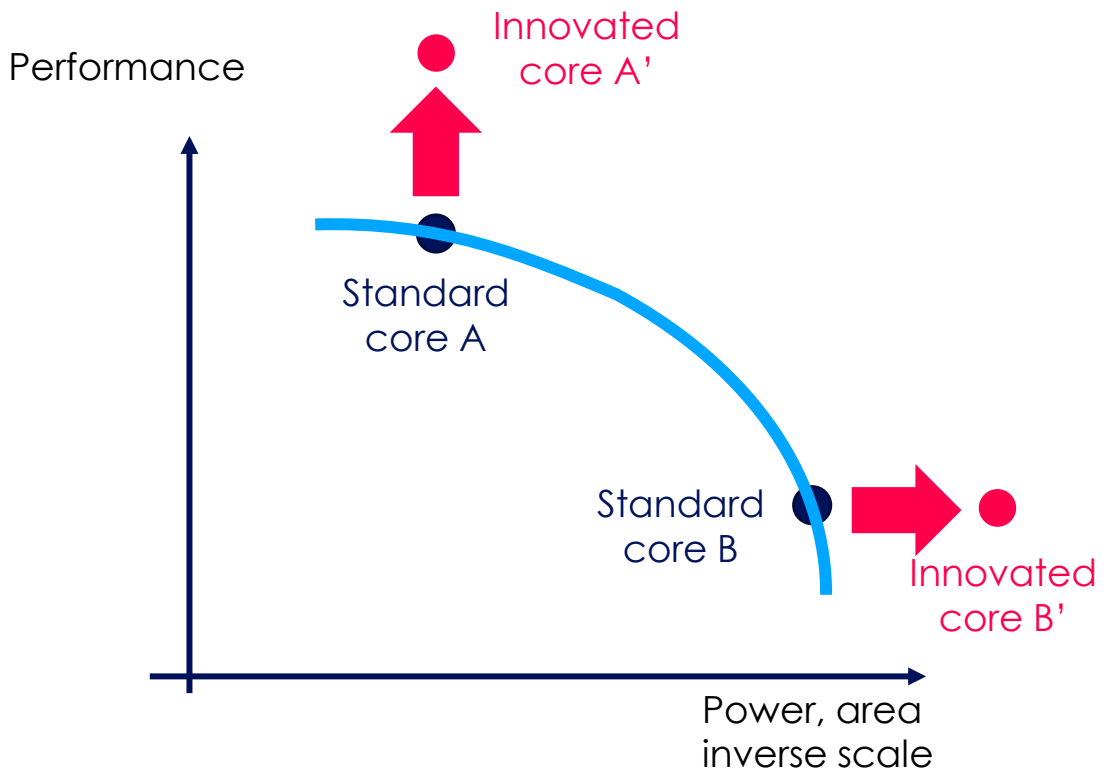
- Scaling is failing
  - Dennard Law stopped
  - Moore's law ending
  - Processor design relying on more cores & bigger caches now less viable due to rising cost-per-gate
- Need for architectural innovation
  - Domain-specific compute
  - Heterogenous architecture
  - HW/SW co-design
- "**Design for Differentiation**"
  - Codasip uniquely capable of enabling this



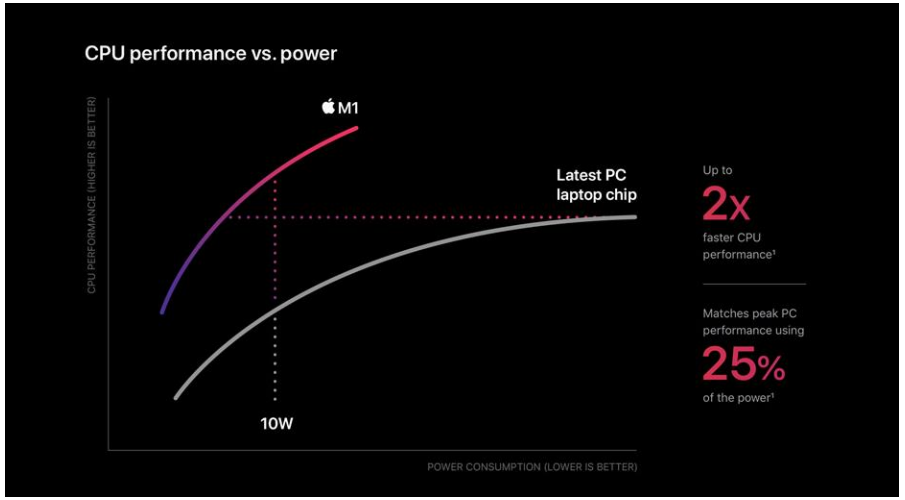


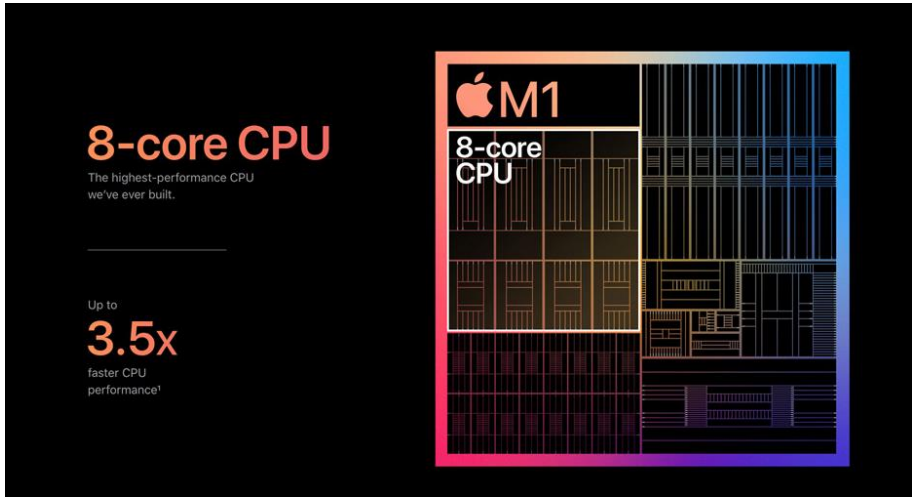
Design Through Differentiation

- Do not rely on Moore's Law or Dennard Scaling
- Instead, improve performance & area by targeting design to application
- Standard cores = single PPA
  - Designed to suit "typical" requirements
  - But each application domain is different
  - Standard solutions = making compromises
- Custom cores = the PPA *you* need
  - Optimal core for *your* application
  - Architecture license: customize both ISA and μArchitecture



It is not just us saying this…





- But that is an Arm architecture license

☹ Proprietary
☹ License is VERY expensive
☹ "High barriers" = huge, expensive team

- What if you want to do it with RISC-V?

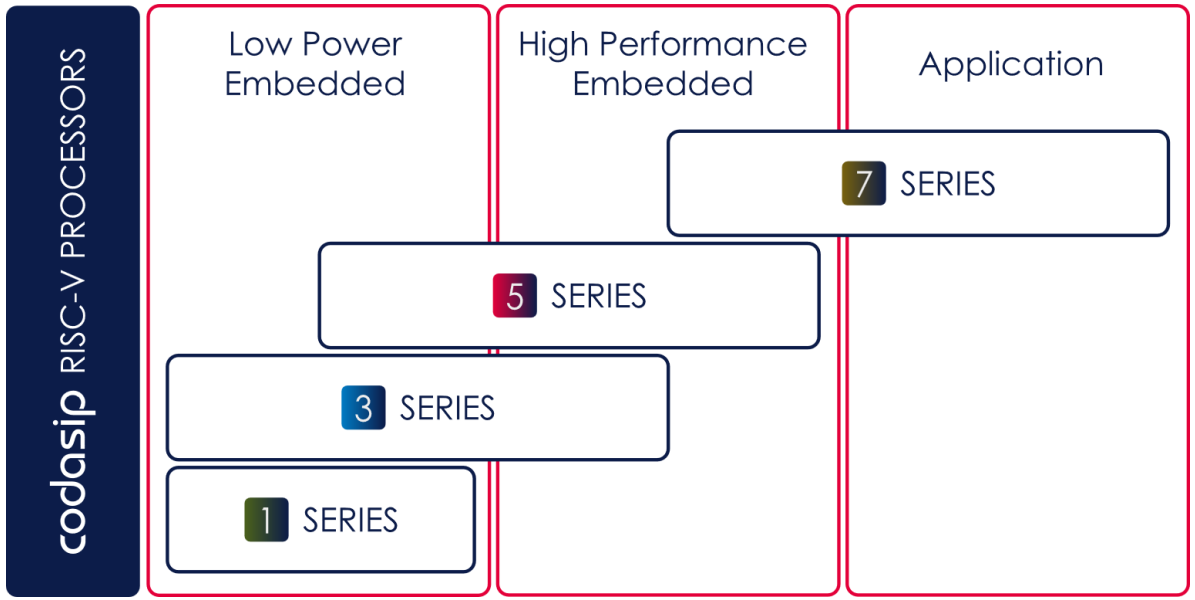
☺ Open standard
☺ Rich eco-system
☹ But still needs a skilled team

- Codasip adds

☺ Architecture license
☺ Studio = Easy, efficient path to modify & customize with small team

Starting Point: Industry Leading Processors

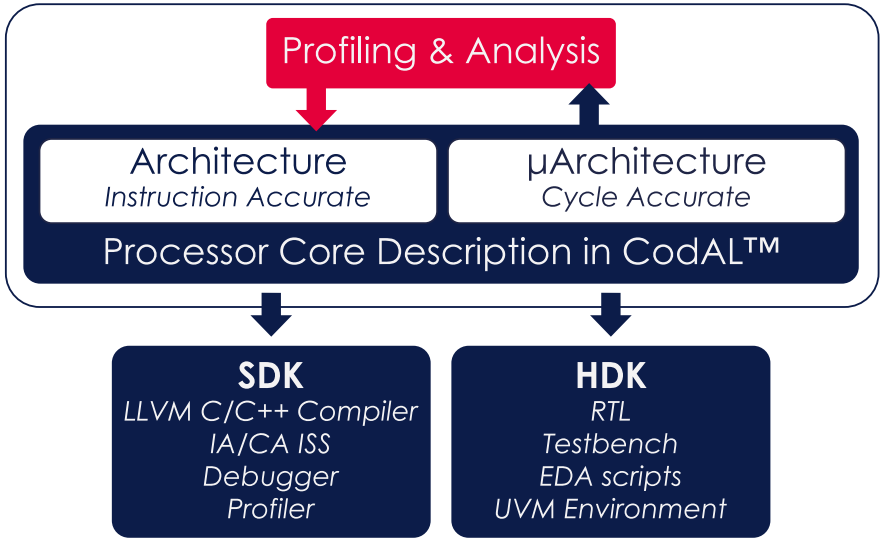
- High Performance
  - Best-in-class verification
  - Tape-out quality, silicon proven
- Processors fully RISC-V compliant
  - RISC-V privilege specification
  - RISC-V debug specification
  - Third-party tools + ecosystem
- Wide range of extensions
  - A, F, D, C, B, P…



Then Differentiate with Codasip Studio

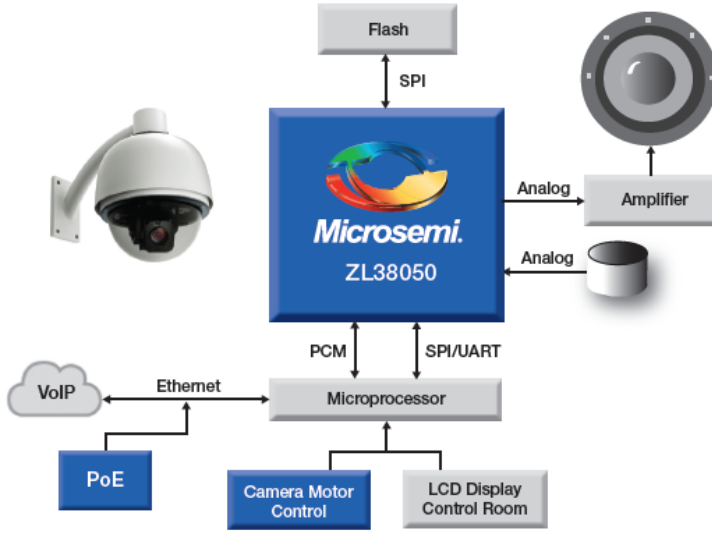
- Customize Codasip RISC-V cores with Codasip Studio
  - Modify both ISA and microarchitecture
  - In CodAL architecture description language
  - Without any architecture license restrictions
- ~3x efficient than traditional RTL approach
- Deliverables generated from a single description
  - HW design, UVM, debugger etc.

Start with proven Codasip IP
or modify open-source RISC-V
or design your own core from scratch



Case Study: Microsemi

- Audio Equalization algorithms
- Requirements
  - Low cost, low power
  - Creating derivative designs
  - Replace Cortex-M core
- Design exploration with Codasip Studio
  - Start with a standard RISC-V core



Microsemi

- Results
  - Performance **56.24x greater***
  - Code size **3.62x smaller***
  - Gate count 2.43x greater**+**
  - Significant saving in costs by targeting older technology node

***** Compared with original design
+ Power and area dominated by instruction memory
Area saving from code size reduction > gate area growth

Case Study: Mythic

MYTHIC

- Unique core for Analog Matrix Processor (AMP™) M1076
- Customized Codasip L30 core
  - DSP, Bit manipulation, Zero-overhead loops
  - Coprocessor control instructions, custom coprocessor interface
- Significantly smaller, higher performance than traditional design
- Designed in ~half the time

"Codasip gave us the flexibility to create a truly unique RISC-V processor that was specific to our needs. This saved us the effort to build our own processor from scratch and allowed us to fully focus on other critical areas of the product development."

Ty Garibay, VP of Hardware Engineering at Mythic

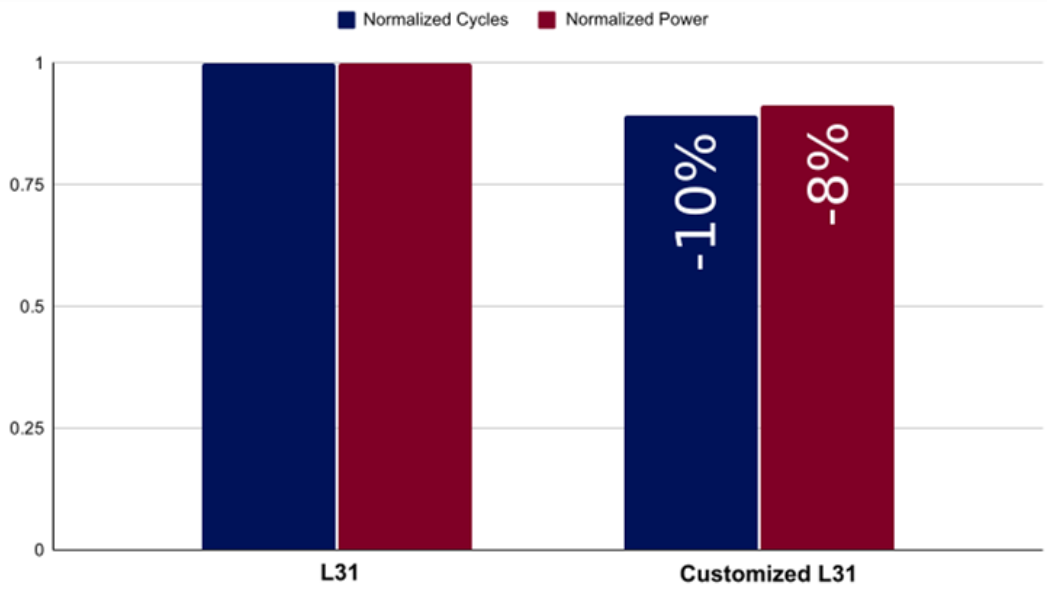
Case Study: AI/ML

- Ported TensorFlow Lite to L31 core
- Optimized for IoT/edge applications
  - Low power / limited memory
- AI handwriting recognition (MNIST)
  - The effect of **2 simple custom instructions**
  - Reduced runtime by **>10%**
  - Reduced power consumption by **>8%**
  - Almost no cost to area **<1 %**

MNIST "Handwritten Digits recognition" benchmark
intelligent label assignment to grayscale 28x28 image

Symbol	Address	Instructions	Instructions Percent	Cycles	Cycles Percent
tflite::reference_integer_ops::ConvPerChannel	36fa6	6572379	86.3 %	9340321	83.9 %
tflite::reference_integer_ops::MaxPool	45e60	412255	5.4 %	710898	6.4 %
tflite::reference_integer_ops::FullyConnected	3e388	158370	2.1 %	236154	2.1 %

Codasip Studio simulator makes it easy to see which are critical algorithms and where to optimize



Conclusion

- In a world where Dennard scaling & Moore's law is ending
  You need to use architectural innovation to succeed
  Design for Differentiation
- RISC-V ideally suited to this
- But you also need verified RISC-V processor to start with and tools to make it efficient and cost-effective to modify to your needs
- **Codasip has this: range of RISC-V cores + Studio tool for customization**

www.codasip.com