OpenHW Group CORE-V Cores Roadmap

Davide Schiavone, davide@openhwgroup.org
twitter: @DavideSchiavo10
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CORE-V Cores

OpenHW Group is specialized in designing open-source, industrial-quality, competitive RISC-V cores

First two cores **RI5CY** and **Ariane** donated by ETH Zurich to take them from academic to industrial grades through
- Improved Documentation and repository structure
- Industrial Verification via the open-source **core-v-verif** project
- Maintenance rules to enable versions compatibility and support

The **CORE-V Family** continues to grow...

May 2022
CORE-V Cores P/N Syntax

CV32E40P

- **FAMILY**: CORE-V
- **WL**: word-length
- **CLASS**: Embedded, Application
- **IDENTITY**: pipe length, version
- **MODIFIER**: special cases

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<table>
<thead>
<tr>
<th>Gate</th>
<th>Purpose</th>
<th>Criteria</th>
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<tbody>
<tr>
<td>PC</td>
<td>Project Concept</td>
<td>Green-light of project concept by TWG</td>
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<td>Project Launch</td>
<td>Full project launch approval by TWG</td>
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<tr>
<td></td>
<td>Plan Approved</td>
<td>Communicate project plan to TWG, (allowing member participation and review)</td>
</tr>
<tr>
<td></td>
<td><strong>Project work</strong></td>
<td></td>
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<tr>
<td>PF</td>
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<td>RTL Freeze checklist or other final final checklist has been completed</td>
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- **Gate**
  - PC: Project Concept
  - PL: Project Launch
  - PA: Plan Approved
  - PF: Project Freeze

- **Purpose**
  - Green-light of project concept by TWG
  - Full project launch approval by TWG
  - Communicate project plan to TWG, (allowing member participation and review)
  - Completion of releasable project content

- **Criteria**
  - Proposed scope, initial view of the components and features, why do this project?
  - Outline of the requirements, features, components, project supporters, risks, high level schedule
  - Project plan full checklist, project methodology, initial agile backlog, requirements specification
  - RTL Freeze checklist or other final final checklist has been completed
TRL Scale

Ideal
Unproven product/technology idea

Basic research
Basic principles observed

Concept formulation
Potential application found and validated. Basic principles have been studied and practical applications identified.

Proof-of-Concept
A crude POC prototype is crafted, demonstrating the core technology (principle) feasibility.

Component and/or Breadboard Lab prototype
Start of engineering R&D: multiple component and subsystems are tested in lab environment.

Subsystems designed and tested in a real life
Validation of the subsystems and engineering units with rigorous testing in relevant (real life) environment.

Functional prototype system (alpha prototype)
Integration of the previously designed sub-systems into a functional ALPHA prototype with first tests.

"Field" demonstration prototype system
Working model or prototype (still ALPHA) demonstrated in relevant environment

Beta prototype (commercial ready system)
A "flight qualified design" embracing DFM approach. Batch production launched and product is being implemented for the intended purpose.

Commercial application. Successful mission
Mass-production. Product/technology is available to all customers.

OpenHW Technology Outputs

OpenHW IP Adopters

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CORE-V Embedded-class Cores
CV32E40P – PF / TRL 5

• 4-stage, in-order, single-issue
• RV32IM[F]CZicount_Zicsr_Zifencei [PULP_XPULP][PULP_CLUSTER][PULP_ZFINX]
• M-mode, CLINT, OBI

• ‘RTL Freeze’ achieved
  • RV32IMC extensions verified
  • Step&Compare with Imperas as reference model (100% coverage)
  • Interrupts and Debug

• Activities on RVFI interface
  • Facilitating sim-based step&compare verification FSM and formal verification

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- Real Time Operating System (e.g. FreeRTOS) capable
  ~600+MHz CV32E4 MCU

- Embedded FPGA fabric with hardware accelerators from QuickLogic

- Multiple low power peripheral interfaces (SPI, GPIO, I2C, HyperRAM, CAMIF, etc) for interfacing with sensors, displays, and connectivity modules

- Built in 22FDX with General Fusion logo

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CV32E40P:v2 – PL / TRL 3

- RV32PULP_XPULP extensions
  - Verification and Reference Model
  - Moving the existing instructions to the RISC-V **custom space**
    - use of custom-0, custom-1, custom-2, and custom-3
  - SW support with upstream GCC and LLVM compiler

RV32F extensions
- Verification

- Project goal: industrial grade (TRL 5)
CI Flow to keep CV32E40P’s sanity

As the RTL changes to the CV32E40P continue (e.g., moving to the custom instruction space, fixing bugs related to RV32F and RV32XPULP instructions), we need to ensure that the verified part of the core (RV32IMC) is kept **formally equivalent** (logical equivalent checking LEC).

To achieve this, we DO NOT allow PPA optimizations or any other NON-LOGICAL-EQUIVALENT modifications to the verified part of the core:

- this avoid compatibility issues and re-run of time-consuming verification routines

This is guaranteed by a **GitHub action running on AWS servers**:

- each PR approved by OpenHW Group staff needs to pass the Logical Equivalent Checking script running on industrial EDA tools
# Maintenance and Compatibility Rules

<table>
<thead>
<tr>
<th>CV32E40P</th>
<th>CV32E40P</th>
<th>CV32E41P/CV32E40</th>
</tr>
</thead>
<tbody>
<tr>
<td>PULP_XPULP</td>
<td>0</td>
<td>PULP_XPULP</td>
</tr>
<tr>
<td>PULP_CLUSTER</td>
<td>0</td>
<td>PULP_CLUSTER</td>
</tr>
<tr>
<td>FPU</td>
<td>0</td>
<td>FPU</td>
</tr>
<tr>
<td>PULP_ZFINX</td>
<td>0</td>
<td>PULP_ZFINX</td>
</tr>
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<td>marchid</td>
</tr>
<tr>
<td>mimpid</td>
<td>0</td>
<td>mimpid</td>
</tr>
</tbody>
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- **Optimization on the frozen parameter set**
- **RTL change on the non-frozen parameter set**
- **Bug fix on the frozen parameter set**
- **New feature (not-LEC)**

- **e.g.** Change in the ISA (USER Mode, PMP, RVB, RVP)
  Performance optimization

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CV32E40S – PA / TRL 2

- 4-stage, in-order, single-issue
- M/U-mode, CLINT, OBI, ePMP, PMA, bus error
- Secure core
  - Reduction of side-channel attacks
- Project goal: industrial grade (TRL 5)
CV32E40X – PA / TRL 2

• 4-stage, in-order, single-issue
• RV32I[M | Zmmul][A]C[X][Zba_Zbb_Zbs|Zba_Zbb_Zbc_Zbs]Zceb_Zce e_Zces_Zicntr_Zicsr_Zifencei_Zihp m
• M-mode, CLINT, OBI, PMA, bus error

• Compute intensive core
  • CV-X-IF interface

• Project goal: industrial grade (TRL 5)
CV32E41P – PC / TRL 2

- 4-stage, in-order, single-issue
- RV32IMCZicount_Zicsr_Zifencei
- [Zce][{F, Zfinx}][PULP_XPULP][PULP_CLUSTER]
- M-mode, CLINT, OBI

- Starting from CV32E40P fork

- Goals:
  - Proof of Concepts to demonstrate the PPA of Zce and Zfinx RISC-V draft ISA extensions

- Project goal: Proof of concept (TRL 3) (next may be TRL 5)
CV32E20 – PC / TRL 2

• 2-stage, in-order, single-issue
• RV32{I,E}[M]CZicount_Zicsr_Zifencei[Zce]
• M-mode, CLINT, OBI

• Low area core
  • Optimized power and area for control-oriented applications
  • Starting point lowRISC Ibex (which started from ETH zero-riscy)
    • Clean-up parameters
    • Aligning IP interface with CV32E40* cores

• Project goal: industrial grade (TRL 5)
CORE-V Application-class Cores
CVA6

• 6-stage, in-order, single-issue
• RV{32|64}IMAC[FD]Zicsr
• M/S/U-mode, CLINT, AXI

• Flexible application core
  • Linux-compatible thanks to MMU
  • 32 or 64 bit (CV32A6, CV64A6) from same RTL (64b from ETH, 32b from Thales)
  • L1 caches

• Project goal: industrial grade (TRL 5)
  • Currently drafting specifications, entry point for next stages
CV64A6 – PA / TRL 4

• Verification
  • RV64GC (RV64IMAFDC), debug, interrupts, privileges... to verify
  • sim-based Step&Compare, formal verification considered
  • RVFI interface

• New documentation
  • reStructured text-based as for the other cores

• FPGA optimizations
  • Target the Xilinx Genesys2, but not a Soft-Core!
CV32A6 – PA / TRL 3

• 32b version support for
  • Pipeline
  • MMU
  • Floating-point
  • Linux

• Verification
  • RV32IMAFC, debug, interrupts, privileges... to verify
  • sim-based Step&Compare, formal verification considered
  • RVFI interface

• PPA optimizations
  • ASIC
  • FPGA (vendor-independent soft-core)
CV32A5 – PC / TRL 3

- 5-stage, single-issue
- RV32I[M][A]
- out-of-order executions
- M, [S,U] Privileged support

- Soft-core
  - Optimized for FPGA
  - Starting from TAIGA from Simon Fraser University

- Project goal: TRL 4
CORE-V SPECs
Specifications for RISC-V COREs
Open Bus Interface (OBI) Spec

• Memory Bus spec for RISC-V cores
  • Handshake based on ARM AMBA AXI
  • Coupled Read-Write channels
  • Easily translatable to ARM AMBA protocols
    • AXI, AHB
  • Based on: https://raw.githubusercontent.com/openhwgroup/core-v-docs/master/cores/cv32e40p/OBI-v1.0.pdf
CV-X-IF Spec

• Bus spec to allow RISC-V cores to offload RV extensions
  • CV32E40X will leverage this interface the most
  • CV32E40P and CVA6 will evaluate it
  • Based on: https://github.com/openhwgroup/core-v-xif

• Verification
  • Formal verification needed to test the spec

• Allows the cores to be agnostic about the custom extension definition
CORE-V Core Logic Blocks

IP surrounding the CORE-V COREs
CV-FPU – PL / TRL 3

• Standalone co-processor that computes floating-point RISC-V RVF and RVD extensions
  • Parts of other projects as
    • CV32E40Pv2, CV32A6, CV64A6

• Possible starting point ETH *fpnew*:
  • Documentation
    • resTructured text documentation
  • Verification stand-alone or as part of the cores

• Project goal: industrial grade (TRL 5)
CV-DBG – PL / TRL 3

• Standalone IP that implements RISC-V Debug Module
  • Debug Transport Module, and ROM for Execution based debug
  • Parts of other projects as
    • CV32E40Pv2, CV32A6, CV64A6

• Possible starting point ETH riscv-dbg:
  • Documentation
    • resTructured text documentation
  • Verification stand-alone or as part of the cores

• Project goal: industrial grade (TRL 5)
CV-VEC – PC / TRL 3

- Datapath extensions that compute vectorial instructions based on RISC-V RVV extensions
- Starting point ETH ara
  - RVB vector extensions and mixed-precision
  - SW support for ML applications
  - Implementation in Globalfoundries 22FDX
  - Support for CV64A6
- Part of OpenHW Accelerate research program with Mitacs, CMC Microsystems, Polytechnique Montréal & ETH Zurich – TRL 4
• **OpenHW Group** is a not-for-profit, global organization driven by its members and individual contributors where HW and SW designers collaborate in the development of open-source cores, related IP, tools and SW such as the **CORE-V** Family of open-source RISC-V cores.

• OpenHW Group & CORE-V Family of open-source RISC-V cores for use in high volume production SoCs
  - Visit the [OpenHW CORE-V Cores GitHub repository](#) and contribute
  - Learn more at [OpenHW TV](#)

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