State of the Union
&
The Road Ahead

Spring 2022 RISC-V Week

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CTO, RISC-V

What we will discuss today

- 2021
- How we did it?
- 2022


2021
RISC-V®

More than 12,000,000,000 RISC-V cores deployed for profit!

16 ratified ISA Specifications
Consisting of 44 Extensions!

10 Committees,

17 SIGs

19 Task Groups

How we did it?

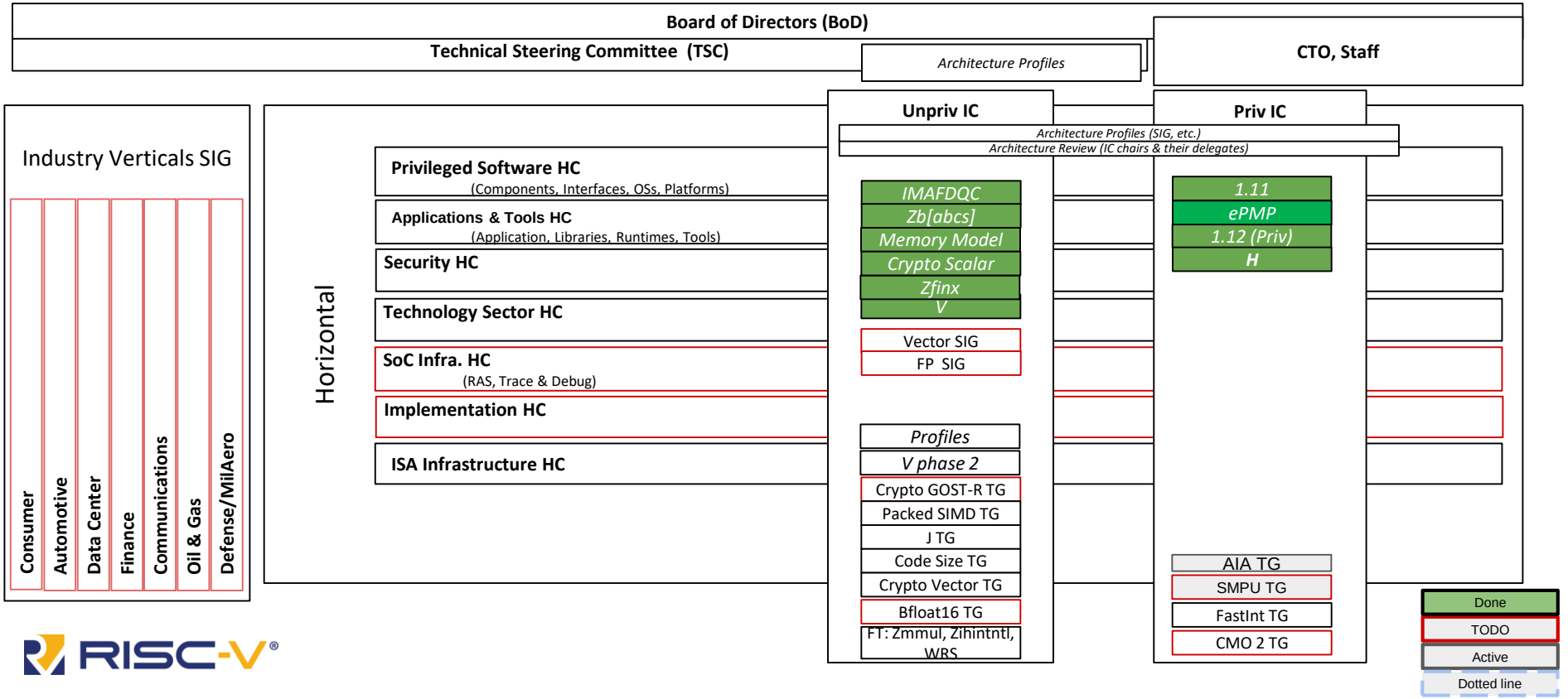

Prioritization
Scalable Organization
Continuous Improvement
PROGRESS!!
Acceptance Criteria
Contributor Culture
Leadership

Why RISC-V?

- Cost
- Flexibility
- Ecosystem
- Our position in History
- EDA Renaissance
- Pride of Ownership


2022
RISC-V®

Technical Organization

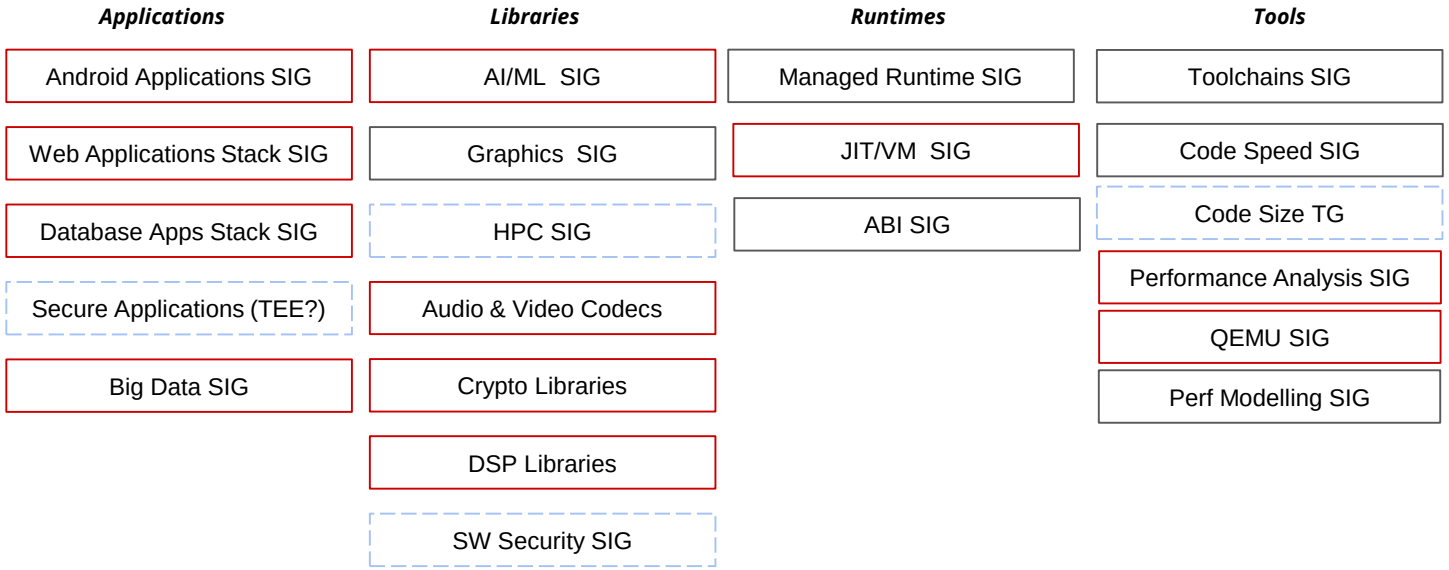


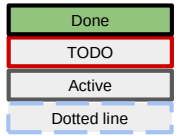
Privileged Software HC

Components	*Interfaces*	*Operating Systems*	*Platforms*
Hypervisors SIG	Plat & FW Services SIG	Operating Systems SIG	Platform SIG
Platform Security SIG	psABI TG (2022)	Android SIG	OS-A SEE TG
Unified Discovery TG	UEFI VTG	Linux/Rich OS SIG	OS-A PlatformTG
IOPMP TG	SBI VTG	RTOS SIG	OS-A PCT TG
AIA TG	ACPI SIG	Distro Tools SIG	
IOMMU TG	SBI SIG		RVM-CSI TG
Secure Boot TG	AP-TEE TG		RVM-CSI PCT TG
PLIC VTG			

Done
TODO
Active
Dotted line

Applications & Tools HC





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SOC Infrastructure HC

- IOMMU TG
- IOPMP TG
- SMPU TG
- TODO
  - Strategy
  - Platform Interrupts
  - Power Management Infrastructure

Debug & Trace SIG

- E-Trace Code
- Debug 0.1X
- Debug revision TG
- E-Trace Data TG
- Nexus TG

RAS SIG

- Functional Safety SIG
- QOS SIG
- E2E Data Integrity SIG
- Error recording, reporting, isolation SIG
- TODO
  - Diagnosability
  - Recoverability
  - Data poisoning containment
  - PCIe error reporting

Security HC

- Crypto Vector TG
- Crypto GOST-R TG
- Security Model TG
- Security Response SIG
- Blockchain SIG
- Control Flow Integrity SIG
- Microarchitecture Side Channel SIG

Trusted Computing SIG

- AP-TEE TG
- Secure Boot TG

Memory Safety SIG

- IOPMP TG
- SMPU TG

Done
TODO
Active
Dotted line

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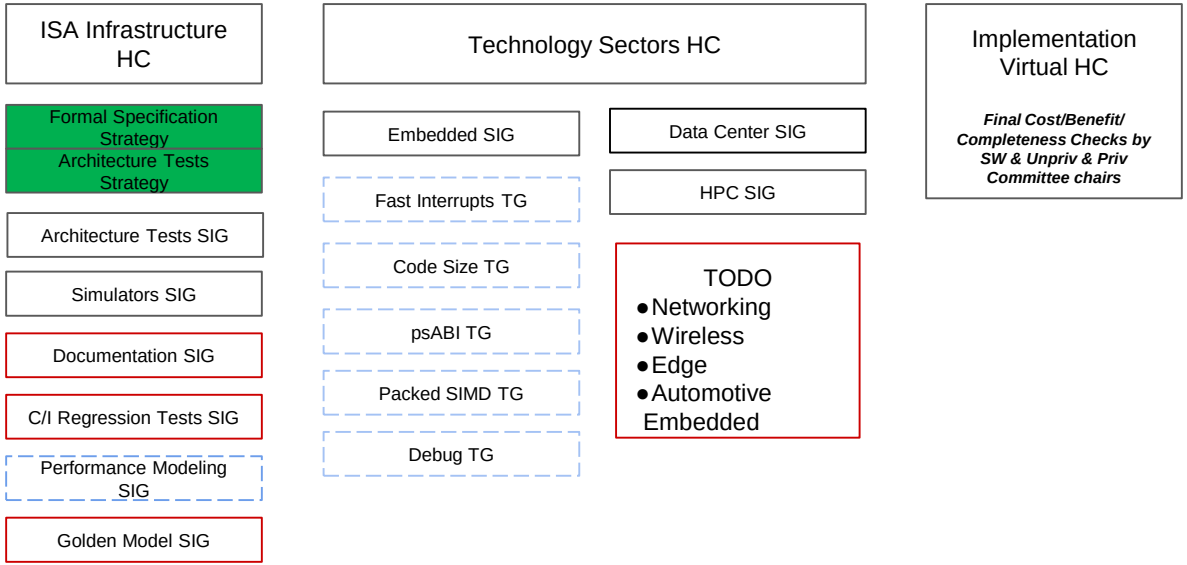

ISA Infrastructure HC
Formal Specification Strategy
Architecture Tests Strategy
Architecture Tests SIG
Simulators SIG
Documentation SIG
C/I Regression Tests SIG
Performance Modeling SIG
Golden Model SIG
Technology Sectors HC
Embedded SIG
Fast Interrupts TG
Code Size TG
psABI TG
Packed SIMD TG
Debug TG
Data Center SIG
HPC SIG
TODO
●Networking
●Wireless
●Edge
●Automotive Embedded
Implementation Virtual HC
Final Cost/Benefit/ Completeness Checks by SW & Unpriv & Priv Committee chairs
Done
TODO
Active
Dotted line

Backlog

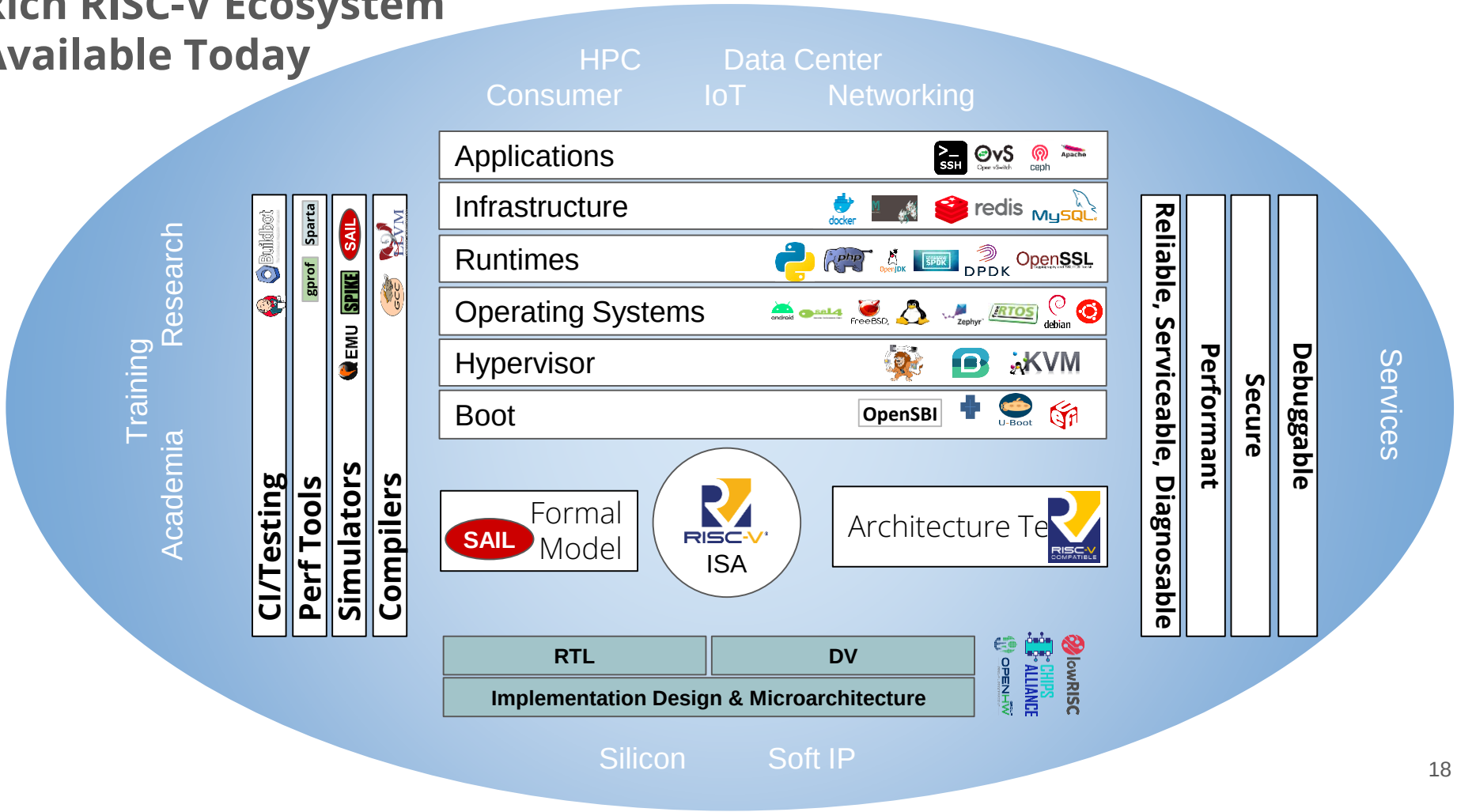
- Profiles
- Platforms
  - Supervisor Execution environment
    - Dependencies: Discovery, Debug, AIA, PLIC, IOMMU, ACLINT, CLIC, EABI, psABI, Watchdog, Arch Test Requirements
- ISA extensions
  - CSR, P, Zc, Zvfh, AIA, bfloat16, security, crypto vector, priv leftovers, Fast Interrupts
  - Never ratified but widely used: Ztso, PLIC, Zicntr, Zihpm

Beyond the Backlog

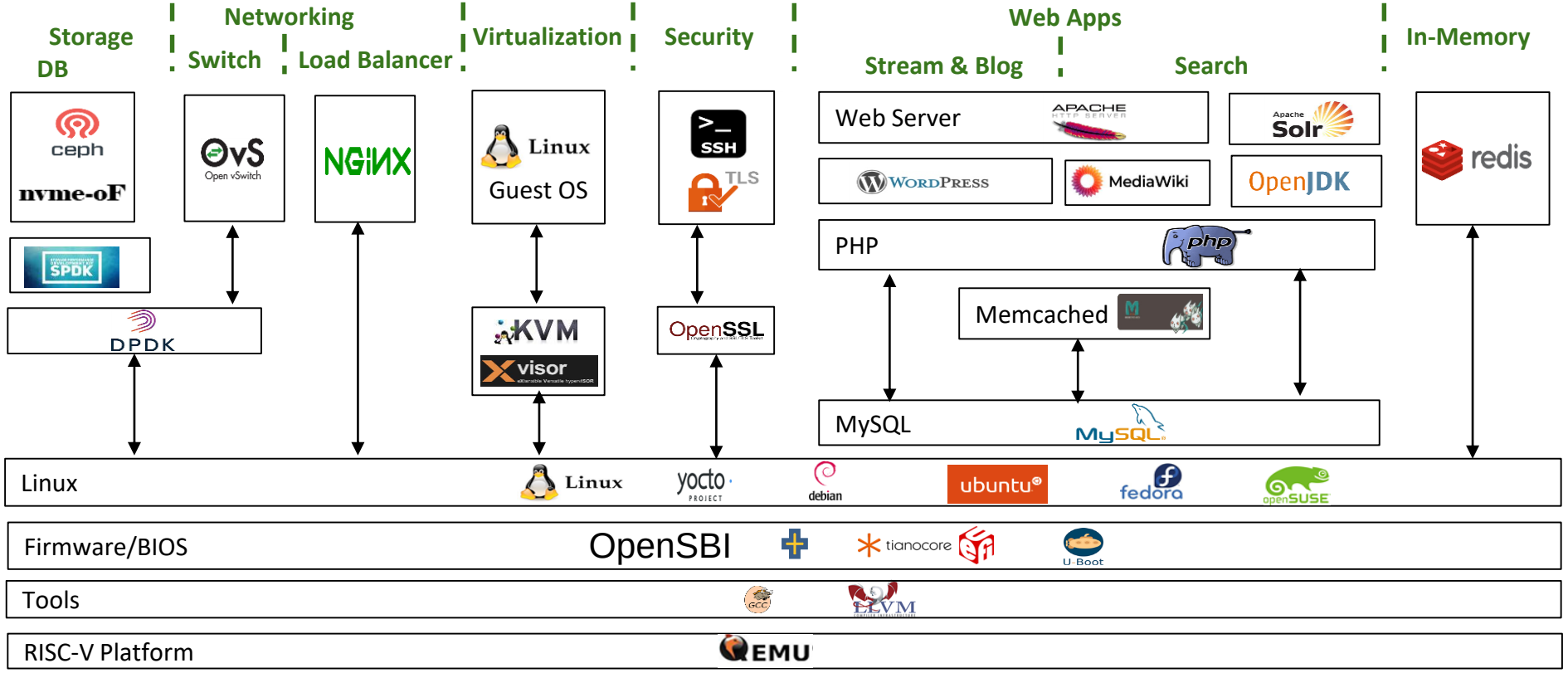
- Automotive
  - AGL & Yocto & Realtime
  - Functional Safety (ASIL, ISO 26262)
- Datacenter
  - Databases
  - Accelerators
    - Graphics & ML/AI/NLP
      - Matrix Ops
  - Emulation Support
    - x86, Arm
  - Virtualization
  - Smart NICs

- ISA Gaps
  - RV32E, RV64E, RV128I
  - Software Ecosystem Libraries
  - Android
- Security
  - uArch
  - Robustness
  - Security Model
  - Ecosystem
- Ecosystem
  - 3rd party ISVs (e.g. VMware or OracleDB)
  - Libraries (security, graphics, etc.)
  - Distros

Rich RISC-V Ecosystem Available Today



Software Stack Examples



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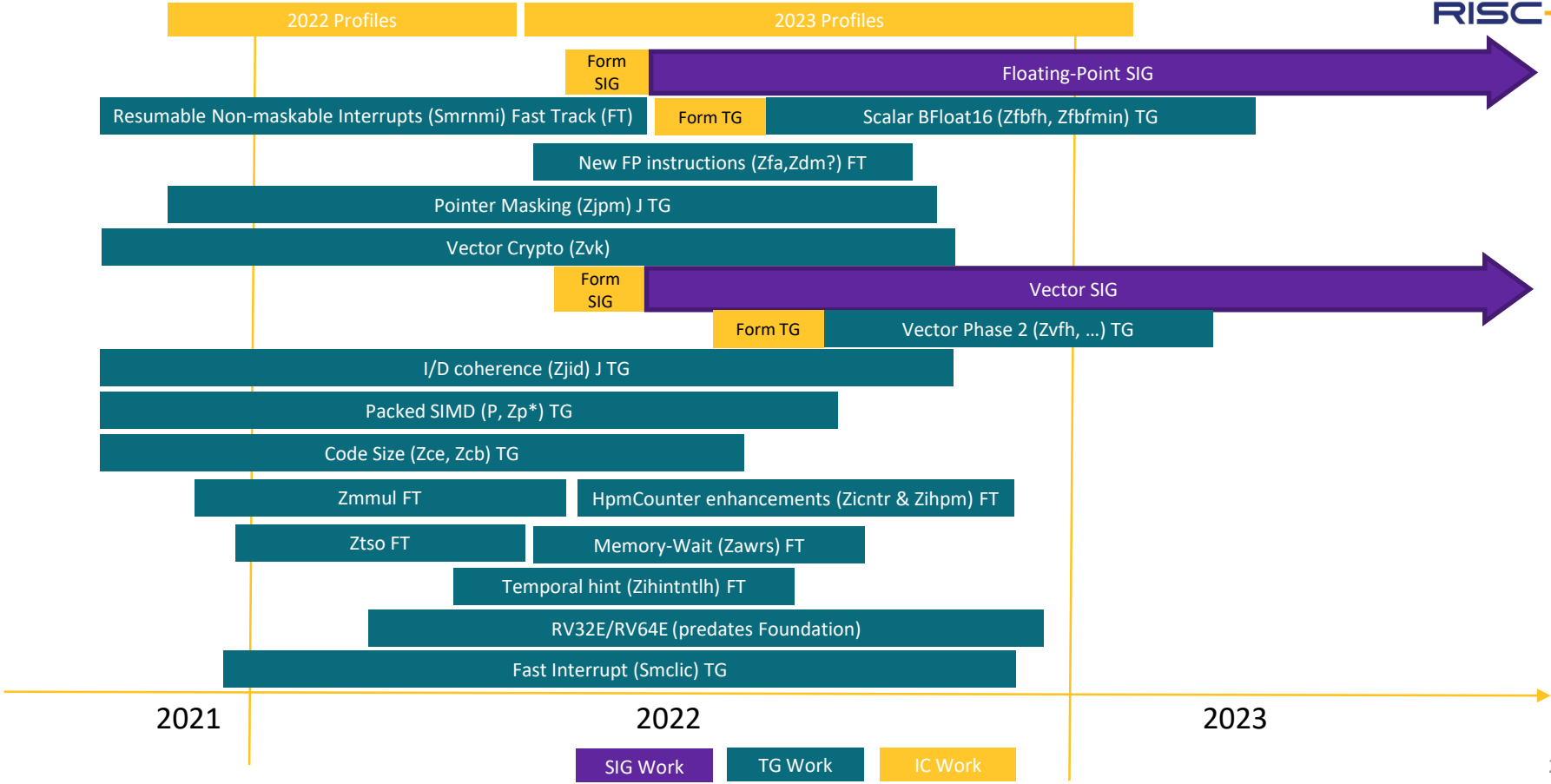
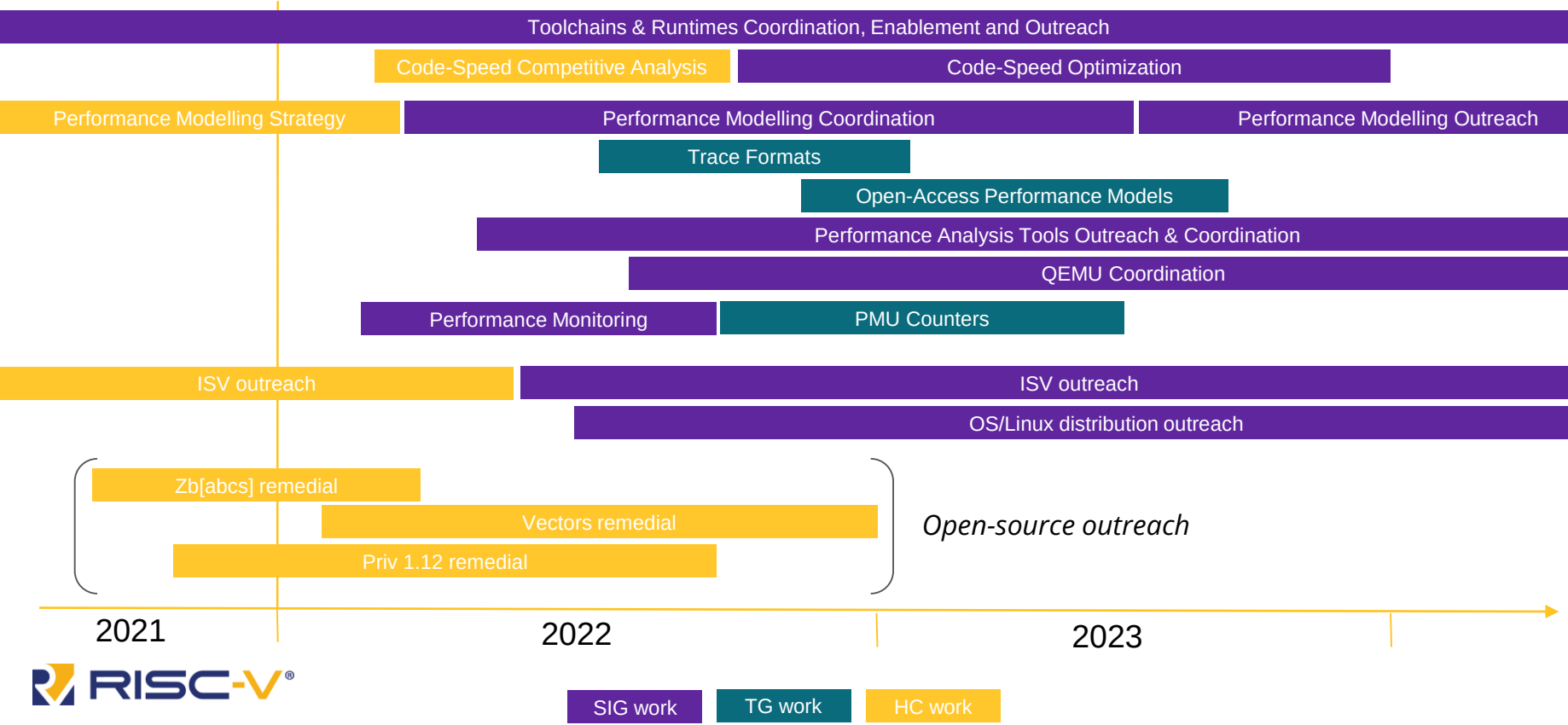
Roadmaps

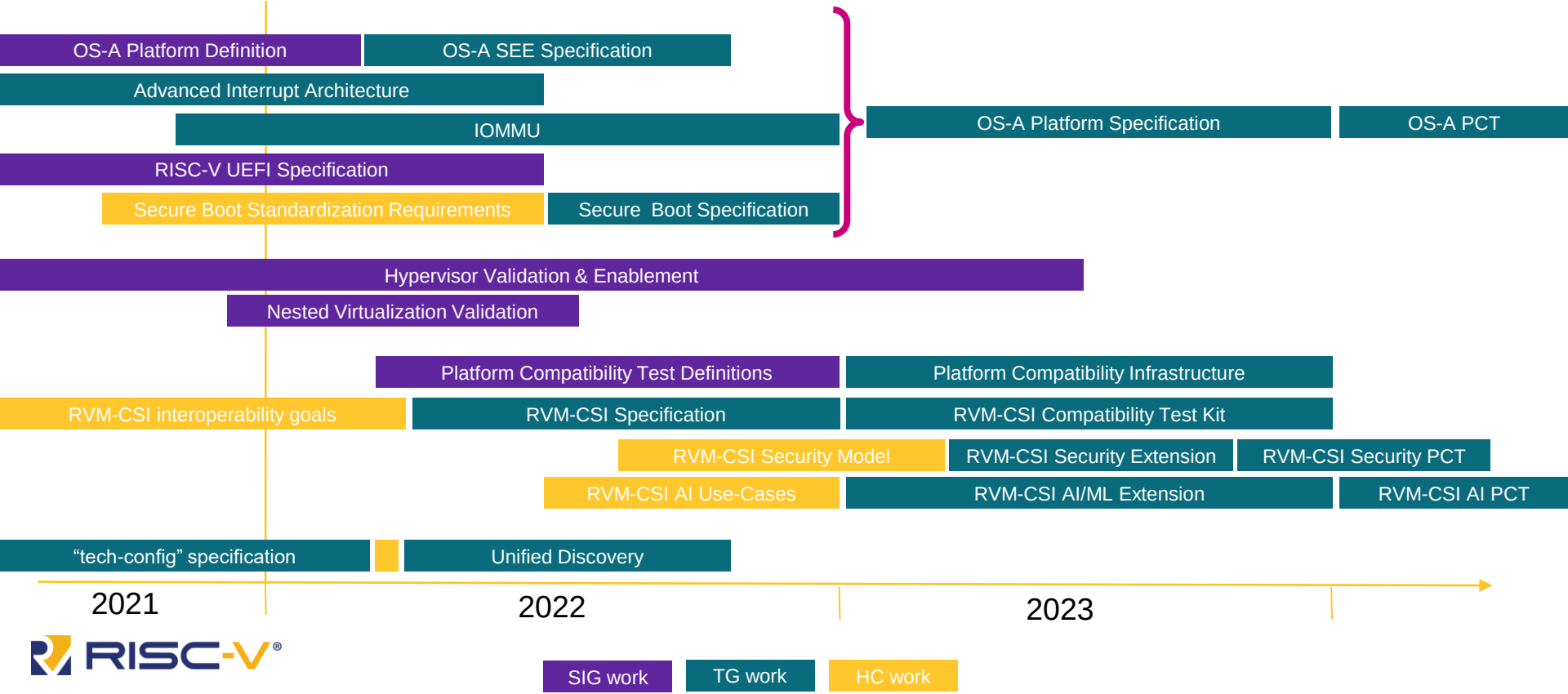
ISA Committees Roadmap (Priv & Unpriv)



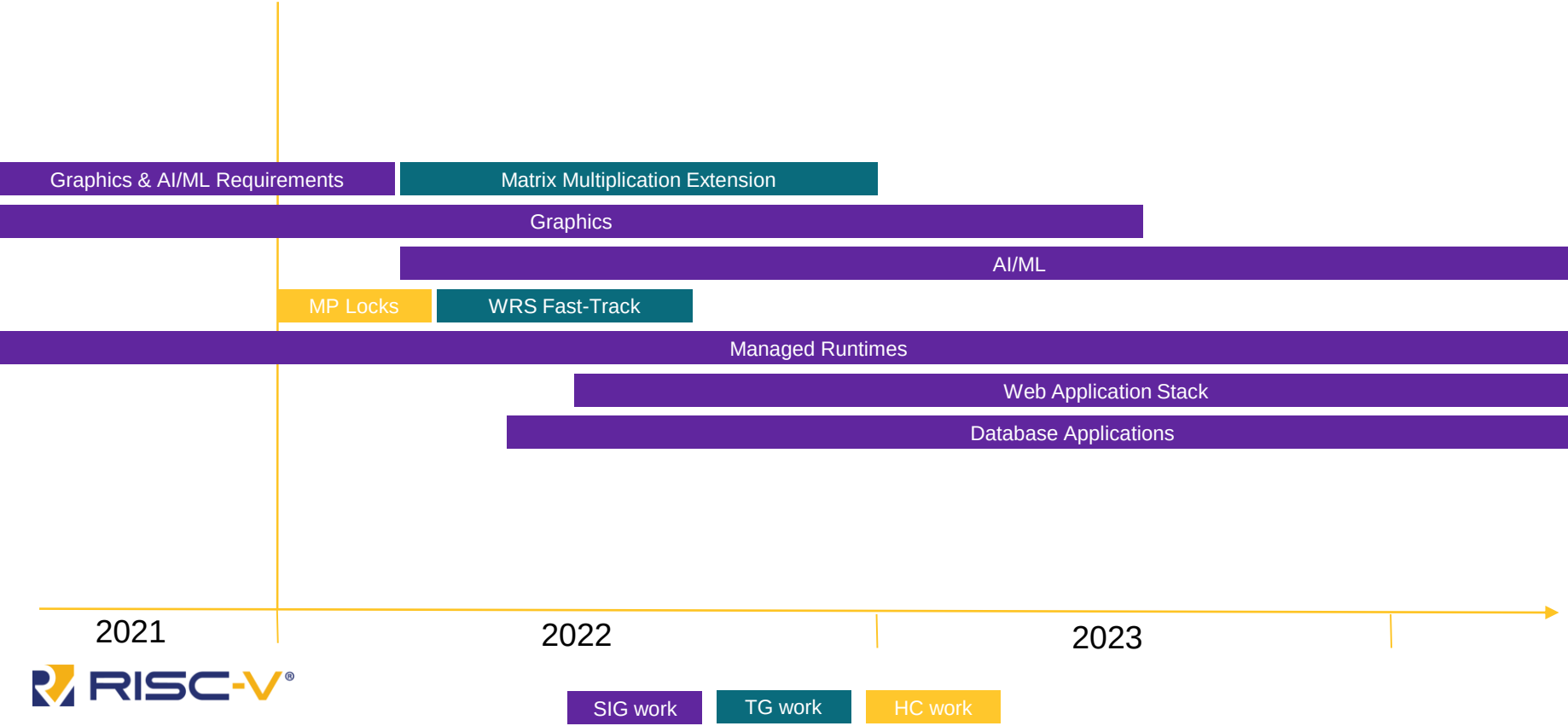
Roadmap: Tools & Performance



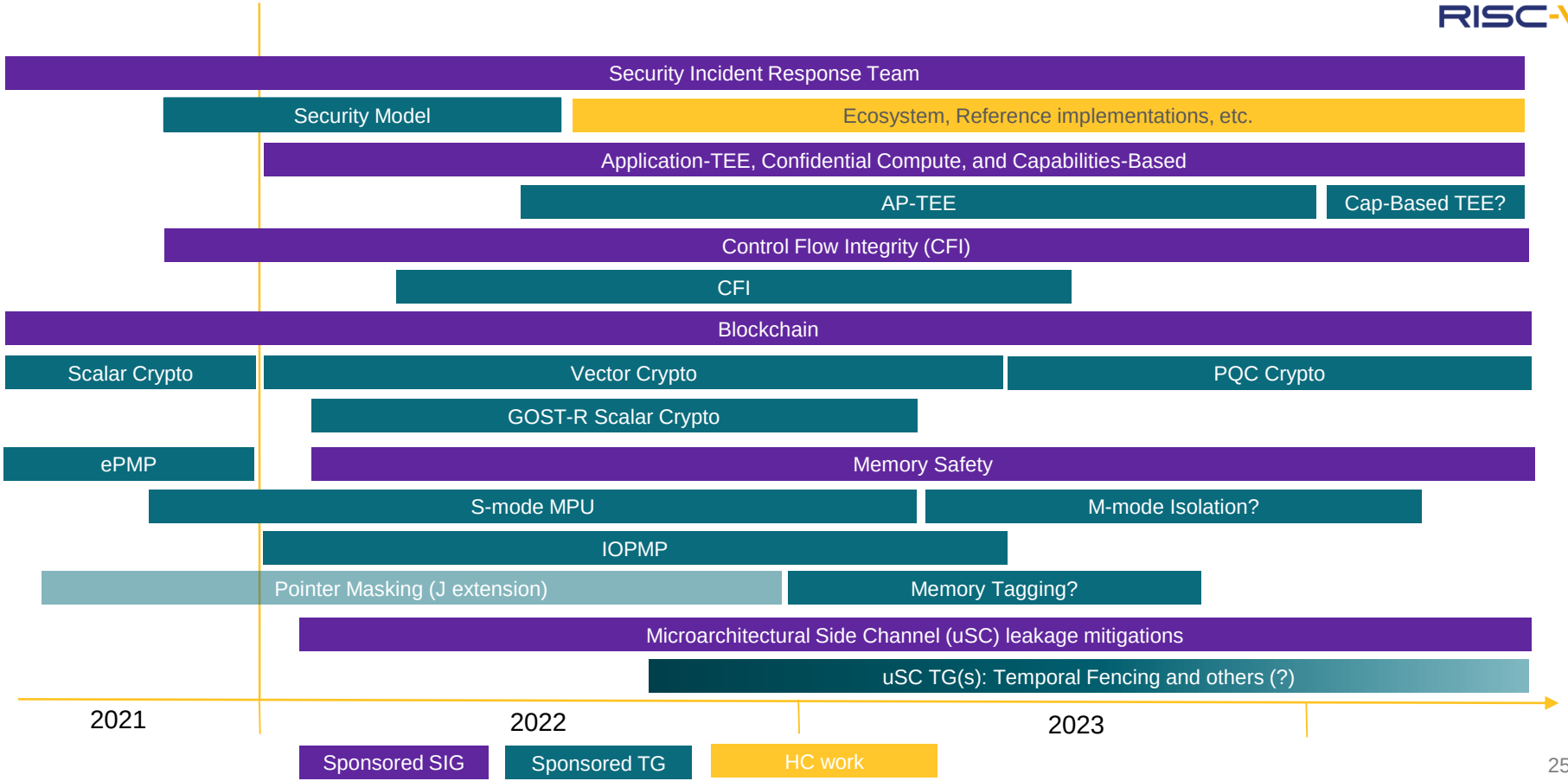
Roadmap: Platforms



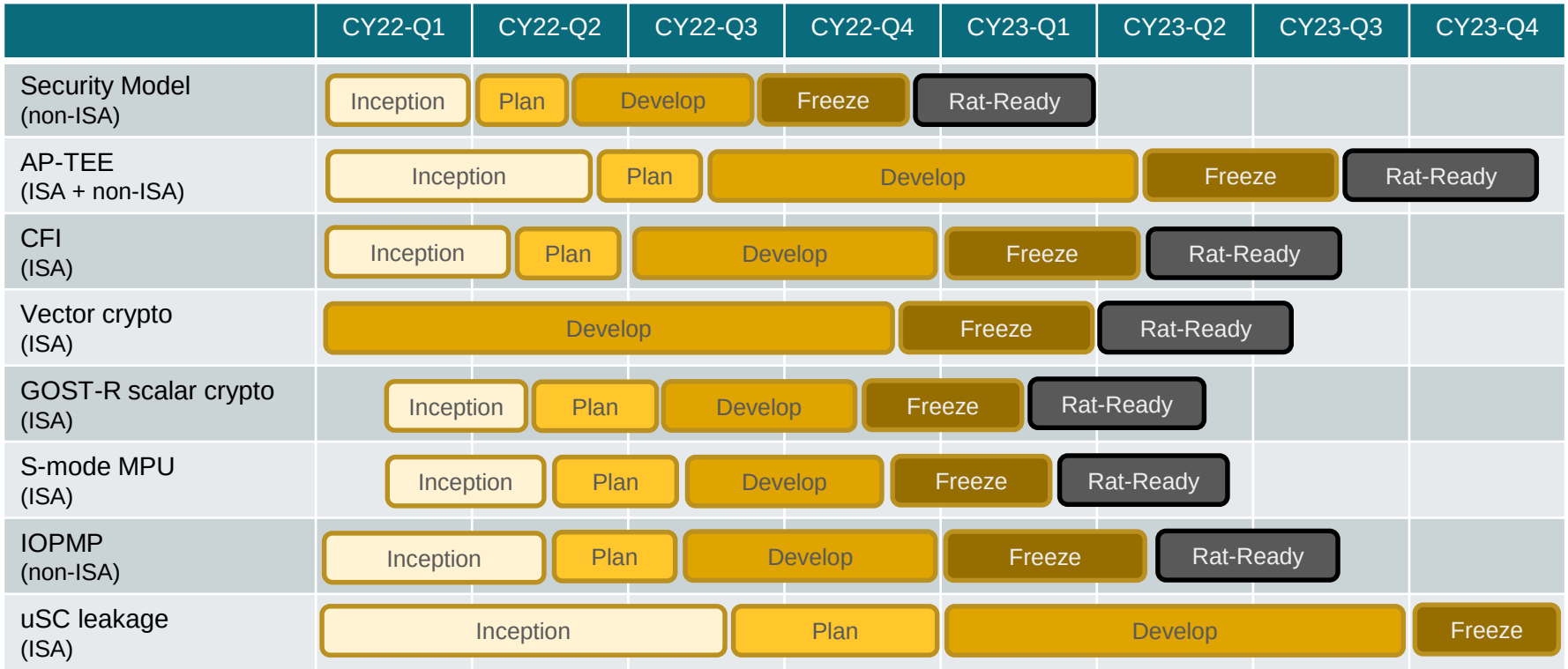
Roadmap: Applications



Security HC - Roadmap



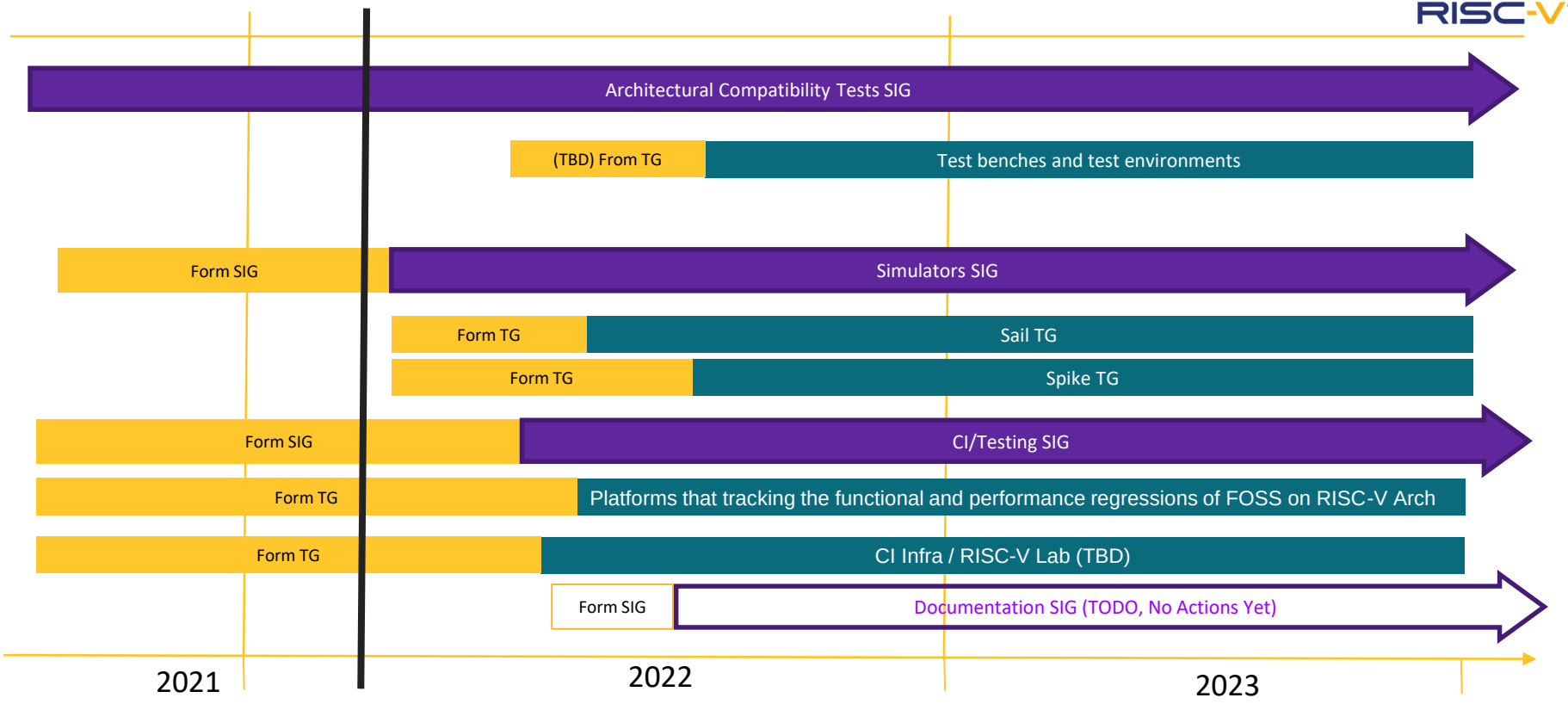
Security Planned Specifications



SoC HC - Roadmap

	CY22-Q1	CY22-Q2	CY22-Q3	CY22-Q4	CY23-Q1	CY23-Q2	CY23-Q3	CY23-Q4
RAS Register interface and signaling (Non-ISA + ISA)		Inception	Plan	Develop	Freeze	Rat-Ready		
Quality of Service (QoS) (Non-ISA + ISA)		Inception	Plan	Develop		Freeze	Rat-Ready	
IOMMU (TG created) (Non-ISA)	Develop		Freeze	Rat-Ready				
SoC performance monitoring and trace (Non-ISA)		Inception	Plan	Develop			Freeze	Rat-Ready

ISA Infra HC Roadmap



SIG Work | TG Work | HC Work | Ratification

Call To Action!

Join!
Contribute!
Make History!
#riscveverywhere

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Thank You!