From Technology to Product
Maturing the RISC-V Ecosystem

Mark Himelstein
Chief Technology Officer, RISC-V International

Dr. Philipp Tomsich
Chief Technologist & Founder, VRULL GmbH

Thursday, May 5th, 2022 | Spring 2022 RISC-V Week
Rich RISC-V Ecosystem
Available Today

HPC
Consumer
Data Center
Networking

Applications
Infrastructure
Runtimes
Operating Systems
Hypervisor
Boot

Reliable, Serviceable, Diagnosable
Performant
Secure
Debuggable

Golden Model
Architecture Tests

RTL
DV
Implementation Design & Microarchitecture

Silicon
Soft IP

CI/Testing
Perf Tools
Simulators
Compilers

Training
Research
Academia

Services

HPC          Data Center          Networking
Consumer          IoT          Networking

OpenSBI

SIPI          Soft IP

Boot
Hypervisor
Operating Systems
Runtimes
Infrastructure
Applications

SAIL

Sparta

gprof
## Addressing stakeholder needs in the ecosystem

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<th>Architecture Development and Co-Optimization</th>
<th>Foundation Software</th>
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<td>Emulators &amp; Simulators</td>
<td>Performance Libraries</td>
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<tr>
<td>Compilers &amp; Debuggers</td>
<td>Managed Runtimes</td>
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<td>Performance Analysis and Modelling Tools</td>
<td>Operating Systems</td>
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### Pre-Silicon Verification

- Software Enablement for Adopters, Independent Software Vendors, and End-Users

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The three principles of the RISC-V ecosystem

Foster adoption and innovation
- Foster a workload-driven evolution of the RISC-V ISA
- Enable the coexistence with vendor-specific extensions

Manage fragmentation
- Standardise the basic platforms
- Enable vendors to gracefully transition from existing non-standard solutions

Deliver optimised software support
- Foster Open-Source Projects, early-adopters, and academia
- Guide the community towards optimisations for RISC-V
Simplified workflow for end-to-end performance

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<th>Performance Modelling</th>
<th>Performance Analysis</th>
<th>Optimised code-speed</th>
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<td>Collaboratively built easy-to-use performance modelling framework for RISC-V</td>
<td>Performance monitoring built into the architecture and enabled by the best-in-class analysis tools</td>
<td>Cross-vendor collaboration provides optimised open source compilers and runtimes</td>
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SPARTA modelling framework

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Modularity + Customisation = Innovation

Modular ISA

Tools and simulators

- Community-adopted policies for including publicly documented vendor-defined extensions in key open-source tools.

- RISC-V Profiles will enhance the usability.

Dynamic discovery

- Multiple mechanisms to select optimised code paths are fully implemented in libraries and the Linux kernel.

- Optimised cache management, cryptography, and string functions are just the beginning.

Vendor-defined (custom) ISA extensions

Created policies for naming of custom instructions to support coexistence across common open-source tools.
OpenJDK19 will natively support RISC-V

RISC-V compiler support merged on March 24th, 2022

https://github.com/openjdk/jdk/commit/5905b02c0e2643ae8d097562f181953f6c88fc89
Android 12 running on RISC-V with optimised AI performance

ClockworkPI announced the DevTerm R-01
A turnkey development kit for educators and hobbyists

Will we see the first RISC-V laptop released in 2022?
Thank you!

- https://lists.riscv.org/g/software
- philipp.tomsich@vrull.eu
- mark@riscv.org