Everywhere

Calista Redmond
CEO, RISC-V International

May 2022
Open source and collaboration are strategic to software and hardware across industries and geographies.
This is our time.
RISC-V empowers our community to seize growing opportunities
RISC-V CPU core market grows 114.9% CAGR, capturing >14% of all CPU cores by 2025

Nearly 80 billion RISC-V CPU cores by 2025

“The rise of RISC-V cannot be ignored... RISC-V will shake up the $8.6 Billion semiconductor IP market.”
-- William Li, Counterpoint Research

Source: Semico Research Corp, March 2021

Source: Counterpoint Research, September 2021
Nearly a quarter of designs incorporate RISC-V

23% of ASIC and FPGA projects incorporated RISC-V in at least one processor in a 2020 study.

Source: Tech Design Forum, November 2020
The definition of open computing is RISC-V

RISC-V is the free and open Instruction Set Architecture

- Simple, modular architecture
- Open collaboration
- Design freedom
- Strategic future
## Disruptive Technology

### Barriers

<table>
<thead>
<tr>
<th>Complexity</th>
<th>Proprietary</th>
<th>RISC-V</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1500+ base instructions Incremental ISA</td>
<td>Simple. 47 base instructions, Modular ISA</td>
</tr>
<tr>
<td>Design freedom</td>
<td>Complex and limited, deep investment</td>
<td>Complete freedom. Flexible, open building blocks</td>
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</table>

### Barriers

<table>
<thead>
<tr>
<th>License fees, Cost of entry</th>
<th>Proprietary</th>
<th>RISC-V</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>$$</td>
<td>Free</td>
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<tr>
<td>Design cost + constraint</td>
<td>$$ – Limited</td>
<td>Free – Unlimited</td>
</tr>
<tr>
<td>Strategic risk</td>
<td>Vendor lock in and dependency</td>
<td>Global community. Invested stakeholders, No vendor lock in</td>
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Unconstrained **Opportunity**
“Deloitte Global predicts that the market for RISC-V processing cores will double in 2022 from what it was in 2021, and that it will double again in 2023, as the served addressable market available for RISC-V processing cores continues to expand.”

December 2021

industry adoption
Investment and traction accelerate in 2022

Intel Corporation Makes Deep Investment in RISC-V Community to Accelerate Innovation in Open Computing

RISC-V welcomes Intel to the Board of Directors to collaborate on RISC-V IP

Intel Creates $1B Innovation Fund To Grow RISC-V Market (And Attract New Foundry Customers) | Karl Freund, Forbes

February 7, 2022

Andes Technology Announces over 10 Billion Cumulative Shipments of Andes-Embedded SoCs and Records All-Time High Annual and Monthly Revenue in 2021

March 8, 2022

We're thrilled to be featured on the @Nasdaq video wall this morning to celebrate our historic moment: a $2.5B valuation from our Series F round! #RISCV #NoLimits

10:02 am - 16 Mar 2022 - HubSpot
Europe invests early as a global open source citizen

EPAC embraced open-source philosophy of give and take, contributing to the RISC-V ecosystem and adding to LLVM compiler database, Linux OS and HPC software such as OpenMP and MPI. Hardware like STX were developed using the PULP platform

— HiPEACINFO 65

The European Commission announced a new European Chips Act of €15 billion in additional public and private investments until 2030. This adds to €30 billion of public investments previously earmarked.

Tue, Feb 8 2022

Intel to spend €17bn on chip mega-factory in Germany… expands manufacturing in Ireland, plus R&D and packaging across Europe

— Tue 15 Mar 2022
• **Esperanto** 1,000-Core RISC-V AI accelerator.
• **Alibaba** RISC-V Xuantie processors with 4 open source cloud and edge processors
• **Imagination** RISC-V CPU family, for discrete and heterogeneous computing
• **Seagate** hard disk drive controller with high-performance RISC-V CPU.
• **Ventana** performance chiplet approach to data center SoC design
• **Intel** Nios processor based on RISC-V, designed for performance.

RISC-V CPU core market will grow 115% CAGR, capturing >14% of all CPU cores by 2025
– Semico Research, December 2021
Communication AI SoC RISC-V designs will grow 21.2% CAGR from 2019-27

- Semico Research, December 2021

- **Andes** RISC-V processor adopted by SK Telecom for AI products.
- **Alibaba** supporting Android 12 on their 64-bit RISC-V core emulated in QEMU
- **Sipeed** RISC-V chip runs Android 10, RV64 phone coming next
- **Alibaba** ported TensorFlow Lite for AI image, audio, and optical in smart devices.
- **Google** Pixel 6 Titan M2 RISC-V processor, with extra speed and memory, more resilient to advanced attacks.
- **MobileEye** vision-based advanced driver assist systems chips capable of 176 trillion ops per second with 12 RISC-V CPU cores.

- **Andes** ISO 26262 Functional Safety ASIL D Dev Process Certification for RISC-V embedded automotive safety with Andes processors

- **Imagination Technologies** GPU linked by a RISC-V core for ASIL-B level designs with ISO 26262 safety critical certification.

- **IAR Systems** extended functional safety of its Embedded Workbench sw tool chain to the RISC-V core of NSITEXE, subsidiary of automotive leader Denso.

- **Europe GaNext** simplifies power converters with GaN power semiconductors with better efficiency and compactness for EV chargers.

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2020 RISC-V automotive opportunity 4M cores; growing to 150M cores in 2022 and 2.9B cores by 2025.

- Deloitte, December 2021

RISC-V will capture 10% of the Automotive market by 2025

- Counterpoint, September 2021
Consumer, IoT devices

- **Huawei** Hi3861 RISC-V board for Harmony OS developers for IoT
- **Zepp Health** / Huami wearable manufacturer OS supporting RISC-V Reference Models for RISC-V P extension
- **GreenWaves** ultra-low power GAP9 hearables platform for scene-aware and neural network-based noise reduction.
- **RIOS Lab** announced PicoRio, an affordable RISC-V open source small-board computer.
- **SiFive** world’s fastest development board for RISC-V Personal Computers.

RISC-V will command 28% of the IoT market by 2025

- Counterpoint Technology Market Research, September 2021
RISC-V-based AI SoCs will grow **73.6% CAGR to 25B units and $291B in revenue by 2027**

- **Alibaba Cloud** tops MLPerf Tiny v0.7 Benchmark with its IOT processor
- **StarFive** released the world’s first RISC-V AI visual processing platform
- **Andes** released superscalar multicore and L2 cache controller processors.
- **NVIDIA CUDA** support on Vortex RISC-V GPGPU enables scaling from 1-core to 32-core GPU based on RV32IMF ISA with OpenCL 1.2 graphics API support.

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- Semico Research, December 2021
Edge Computing

- **Fraunhofer** ported Tensorflow lite to their RISC-V processor core for Edge AI applications incl sensor data evaluation, gesture control, or vibration analysis.

- **Seeed Studio**’s new Sipeed MAIX, a RISC-V 64 AI board for Edge Computing makes it possible to embed AI to any IoT device.

- **Micro Magic** announced an incredibly fast 64-bit RISC-V core achieving 5GHz and 13,000 CoreMarks at 1.1V.

- **Western Digital** SweRV Core enables spectrum of compute at the edge.

- **Microchip** released the first SoC FPGA development kit based on the RISC-V ISA.
- **E4 Monte Cimone Cluster** along with DEI-UNIBO contributing to architecture, software, and integration.

- **European Processor Initiative** RISC-V accelerator with first chip Sep 2021

- **Technical University of Munich** (TUM) quantum cryptography chip for quantum computing security demands

- **Tactical Computing Labs** HPC-centric software test suite for GCC and LLVM

- **Cortus** is developing a high-performance RISC-V Out-of-Order processor core for the European eProcessor project.

- **De-RISC** HW-SW platform for multi-core RISC-V SoC for safety critical aerospace

Johanna Baehr of TUM heads a team that has hidden four hardware Trojans on this chip - malicious functions that are integrated directly into the circuits.
Rich RISC-V Ecosystem Available Today

HPC  Data Center  Networking
Consumer  IoT

Applications
Infrastructure
Runtimes
Operating Systems
Hypervisor
Boot

OpenSBI

Reliable, Serviceable, Diagnosable
Performant  Secure  Debuggable

Services

RISC-V

Golden Model
Architecture Tests

SAIL Model

RTL  DV
Implementation Design & Microarchitecture

Silicon  Soft IP

Training  Research

Academia

CI/Testing  Perf Tools  Simulators  Compilers

HPC          Data Center          Networking
Consumer          IoT          Networking

Applications
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Academia
More than 2,700 RISC-V Members across 70 Countries

- 106 Chip
  - SoC, IP, FPGA
- 3 Systems
  - ODM, OEM
- 3 I/O
  - Memory, network, storage
- 13 Industry
  - Cloud, mobile, HPC, ML, automotive
- 18 Services
  - Fab, design services
- 109 Research
  - Universities, Labs, other alliances
- 52 Software
  - Dev tools, firmware, OS
- 2k+ Individuals
  - RISC-V engineers and advocates

RISC-V membership rapid growth of 134% in 2021
RISC-V delivers incredible member support

Technical Deliverables
- Technical governance
- Build technical deliverables
- Guide strategic technical Work groups

Compatibility & Verification
- Profiles & Platforms & Architecture
- Compatibility Tests (ACT) & Platform Compatibility Tests (PCT)

Visibility
- Amplify member news, content, and success with press and analysts
- Original content programs
- RISC-V, industry, and regional events

Learning & Talent
- Multi-level online learning
- Connecting universities with labs, tests, and curricula
- RISC-V Training Partners
- Jobs and internships

Advocacy + Alliances
- RISC-V Ambassadors
- Geo and industry alliances
- Local developer groups and events

Marketplace Exchange
- Online marketplace of providers, products, services, and learn
- Technical developer forums
# RISC-V Innovation Roadmap

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<th>Test Chips</th>
<th>Software</th>
<th>ISA</th>
<th>ISA Extensions</th>
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<tr>
<td>Proof of Concept SoCs</td>
<td>IoT SoCs</td>
<td>RV32</td>
<td>Profiles</td>
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<tr>
<td>Minion processors for power management &amp; communications</td>
<td>Microcontrollers</td>
<td>RV32I and RV64I</td>
<td>Packed SIMD</td>
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<tr>
<td>Bare metal software</td>
<td>RTOS, Firmware</td>
<td>Base instructions: Integer, float, double, quad, atomic, and compressed instructions</td>
<td>Advanced Interrupts</td>
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<tr>
<td></td>
<td>Development tools</td>
<td>Priv modes, Interrupts, exceptions, memory model, protection, and virtual memory</td>
<td>Java: ptr masking, I/D synch</td>
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<td>Technical Steering Committee, HPC SIG, GlobalPlatform partnership</td>
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<td>RV32E &amp; RV64E</td>
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<th>2010-2016</th>
<th>2018</th>
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<tbody>
<tr>
<td>ISA Definition</td>
<td>RV32</td>
<td>RV32I and RV64I</td>
<td>Base instructions: Integer, float, double, quad, atomic, and compressed instructions</td>
<td>Architecture Compatibility Framework Trace</td>
<td>Vector</td>
<td>Profiles</td>
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<td>RISC-V Foundation</td>
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<td>Virtual Memory</td>
<td>Vector Half-Precision Floating Point</td>
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**Ecosystem**

- **SIGs:** Security Response, AI, Graphics, Android, Embedded, Datacenter/Cloud, Blockchain, Simulators, Managed Runtimes, Android, Functional Safety
- **Programs:** Dev Board Seed, Development Partners, RISC-V Labs
- **Ecosystem:** RISC-V Security Model, AP-TEE, IOPMP
- **Platform specs:** Platforms, SEE, SBI, ABI, Discovery, Watchdog, ACPI, UEFI
- **SOC specs:** E-Trace, Nexus, IOMMU
- ** ISA Extensions:** Matrix Ops, Crypto Gost
Investments in open source bring a 4x return

EU companies invested €1 billion in Open Source Software in 2018, providing economic impact of €65 - €95 billion, with a cost-benefit ratio of >1:4.

Technical advantage

Lower maintenance costs. Contributing to upstream projects ensures technical elements will be included in future updates without ongoing development costs.

Influence direction. New features come from contributions. To include functionality important to your organization, you need to support active project contributors.

Talent matters

Open source saves time and money. Developers can save ~45 minutes a day with open source. For an organisation of 1,800 people, this can be financial savings of $12.4 million over three years.

Attract, retain, and build technical talent and collaborative culture. 48% of businesses contributed to open source projects to access developer talent. Employees relationships and identify good fits for your company while working on their favorite project.
Build RISC-V into your company strategy, and your personal mission

RISC-V is a community of passionate, dedicated, and invested stakeholders

As individuals
As companies
As universities
As public institutions and non-profits
As nations

As one Global, connected movement
Thank You

@risc_v
@calista_redmond

www.riscv.org

risc-v-international
calistaredmond
Benefits of engaging in RISC-V

- ✓ Accelerate technical traction and insight
- ✓ Contribute technical priorities, approaches, and code
- ✓ Gain strategic and technical advantage
- ✓ Increase visibility, leadership, and market insight
- ✓ Fill and increase engineering skills, retain and attract talent
- ✓ Build innovation partner network and customer pipeline
- ✓ Deepen, engage, and lead in local and industry developer network
- ✓ Showcase RISC-V products, services, training, and resources
### Membership Options

#### Premier Member Benefits
- Board seat and Technical Steering Committee seat included at $250k level
- Technical Steering Committee seat included at $100k level
- Board level includes seat on RISC-V Legal Committee
- Eligible to lead workgroup and/or committee
- Use of RISC-V Trademark for commercialization
- Member logo / name listing on RISC-V website, alphabetical with Premier members
- Solution / Product listing highlighted on RISC-V Exchange, noted with member level
- 4 case studies a year
- 2 blogs per month
- 2 social media spotlights per month
- Spotlight member profile
- Event sponsorship discount

#### Strategic Member Benefits
- 3 Board reps elected for the Strategic tier, including Premier members that do not otherwise have a board seat
- Eligible to lead workgroup and/or committee
- Use of RISC-V Trademark for commercialization
- Member logo / name listing on RISC-V website, alphabetical with Strategic members
- Solution / Product listing highlighted on the RISC-V Exchange, noted with member level
- 1 case study a year
- 1 blog per month
- 1 social media spotlight per month
- Event sponsorship discount

#### Community Member Benefits
- Membership open to academic institutions, non-profits, individuals not representing a legal entity
- No annual membership fee

#### Premier Requirements
- Membership open to any type of legal entity
- $250k Annual membership fee that includes Board seat and TSC seat
- $100k Annual membership fee that includes TSC seat

#### Strategic Member Requirements
- Membership open to any type of legal entity
- Annual membership fee based on employee size
  - 5,000+ employees: $35k
  - 500-5,000 employees: $15k
  - <500 employees: $5k
  - <10 employees & company <2 yrs old: $2k

#### Community Requirements
- Membership open to academic institutions, non-profits, individuals not representing a legal entity
- No annual membership fee
Technical Organization

Board of Directors (BoD)

Technical Steering Committee (TSC)

Architecture Profiles

CTO, Staff

Unpriv IC

Priv IC

Architecture Profiles

Architecture Review (IC chairs & their delegates)

Industry Verticals SIG

Consumer

Automotive

Data Center

Finance

Communications

Oil & Gas

Defense/MilAero

Horizontal

Software HC

(Platforms, Toolchains, Runtimes)

Security HC

RAS HC

Technology Sector HC

SoC Infra. HC

(Trace & Debug)

Implementation HC

ISA Infrastructure HC

Technical Organization

CTO, Staff

Crypto Scalar

SMPU TG

Fastint TG

CMO 2 TG

Vector SIG

FP SIG

V phase 2

Crypto GOST-R TG

Packed SIMD TG

J TG

Code Size TG

Crypto Vector TG

Alt FP TG

FT: Zmin, Zhintnl, WRF

V

Zfinx

Crypto GOST-R

Zb(abc)

Memory Model

IAFDQ

ePMP

1.11

1.12 (Priv)

H

FT: Zmin, Zhintnl, WRF

TODO

Active

Dotted line

Priv IC

AIA TG

DONE
Software Horizontal Committee

Platform HSC
(includes platform specs)
- Config TG
- Hypervisors SIG
  - AIA TG
  - IOPMP TG
  - OS-A Platform SIG
  - RVM-CSI Platform TG
  - OS-A SEE TG
  - OS-A Platform TG
  - OS-A PCT TG

Topics TODO:
- Linux class OSs
- RTOSs
- DMA
- Multi-processing
- JITs
- IOMMU, Buses
- Bootloaders
- Distro coordination/build/rel
- QOS
- Perf monitoring

TGs for specs underway

Toolchain & Runtimes HSC
- psABI TG
- Code Size TG
- HPC SIG
- Managed Runtimes SIG

AI/ML/NLP/Graphics SIG
- Android SIG
- Perf Modeling SIG
- Perf Analysis SIG
- IOMMU TG

AI/ML/NLP/Graphics SIG
- Android SIG
- Perf Modeling SIG
- Perf Analysis SIG
- IOMMU TG

Topics TODO:
- Benchmarks
- Regression test strategy
- Ecosystem changes
- Extensions needed
- Worst Case Execution Time (WCET)
- Spatial & Timing interference
- DSP
- DB & Hadoop et al
- Performance analysis
- Native code
  - GCC
  - LLVM
  - Optimizer
  - Profiler
  - gdb
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<thead>
<tr>
<th>Technology Sectors HC</th>
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<tr>
<td>Data Center SIG</td>
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<tr>
<th>Implementation Virtual HC</th>
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<tr>
<td>Final Cost/Benefit/Completeness Checks by SW &amp; Unpriv &amp; Priv Committee chairs</td>
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<th>Security HC</th>
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<td>Crypto Vector TG</td>
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<td>Crypto GOST-R TG</td>
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<td>Security Model TG</td>
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<td>Trusted Computing SIG</td>
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<td>AP-TEE TG</td>
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<td>Control Flow Integrity SIG</td>
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<td>Microarchitecture Side Channel SIG</td>
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<td>Memory Safety SIG</td>
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<th>ISA Infrastructure HC</th>
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<td>Functional Safety SIG</td>
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<td>QOS SIG</td>
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<td>E2E Data Integrity SIG</td>
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<td>Error recording, reporting, isolation SIG</td>
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<td>Diagnosability</td>
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<td>Recoverability</td>
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<td>Data poisoning containment</td>
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<td>PCIe error reporting</td>
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<td>Edge</td>
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<td>Automotive Embedded</td>
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RISC-V Technical Programs

RISC-V Platform
A common, reusable runtime environment that operating systems and applications can target to improve portability and reuse. Provides interoperability assurance.

RISC-V Profiles
Refers to a base ISA and one or more extensions that are specified as a group so that applications can be compiled once, run on different implementations, and get the same results.

RISC-V Compatible
Architectural Tests created to help ensure that software written will run on implementations that comply with that profile. Branding available for compatibility.

RISC-V Lab
Institutions that host a lab with RISC-V hardware for CI/testing and general availability sandboxing.

RISC-V Development Partner
Recognizes the investment and dedication of organizations making significant technical contributions to RISC-V.

RISC-V Developer Boards
Available to spur innovation, provide hands-on education, and engage early adopters to test and develop.

https://wiki.riscv.org/display/TECH
## Visibility Opportunities

<table>
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<th>Events</th>
<th>Content</th>
<th>Proactive AR / PR</th>
<th>Social</th>
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| RISC-V and Industry events **Local**, regional, and global events  
Speaking opportunities  
Showcase and announce RISC-V solutions  
Networking  
Host your own RISC-V Event | The RISC-V blog program showcases leadership, industry commentary, and technical information.  
To submit content, fill out the [Google Form](#) or email content@riscv.org. | Share member and community news “In the News”  
RISC-V provides quotes for member press releases  
Participate in media panels and interviews | **Twitter**  
**LinkedIn**  
Members submit original content for posting on RISC-V social channels  
Members and the community submit content for re-sharing.  
Amplify member announcements via social  
To submit content, fill out the [Google Form](#) or email content@riscv.org. |

### Engage!
- RISC-V Marketing Committee  
- RISC-V Events Committee  
- RISC-V Content Committee

### Exchange
- Promote member and community solutions  
- Connect developer community

### Case Studies
- Elevate technical conversations to business objectives and challenges, showing adoption of RISC-V.  
Case studies on riscv.org are shared to media channels and analysts.
Community and Learning

**Alliances**

Alliances are technical and strategic relationships across industries, geographies, and technical domains providing mutual community support.

**Ambassadors**

RISC-V Ambassadors are the technical experts and leaders in the RISC-V community. They work together with RISC-V to help drive our global momentum and adoption of RISC-V technologies.

Meet the Ambassadors

**Learn**

There are many materials to help you learn or teach RISC-V, including trainings, published books, technical and scholarly articles written around the world, and a lengthy collection of open educational materials provided by our community.

University resources

Online Courses

Training Partners

**Talent**

RISC-V paid Mentorships are offered quarterly with projects submitted by members and open applications to the community.

Looking for a job or want to post a RISC-V related job? Check our the Careers page!

Open Hardware Diversity Alliance bringing together the open hardware community to support the professional advancement of underrepresented individuals in open source hardware.

Travel scholarships offered for RISC-V Summit.

Engage!

RISC-V Academia + Training SIG