Agenda

- Why RISC-V goes BIG
- Who is Andes
- Andes RISC-V Core Features
- Andes RISC-V Roadmap
- Andes RISC-V environment
RISC-V Powering Industry Leaders

Mobile
Mobile AP
TDDI
Billions shipment of connectivity, touch, and sensor hub.

IoT MCU
Performance, safety and customization enabling innovative ASSP MCU
Renesas

AI
Configurable and efficient core to power high-performance AI
SK telecom

5G
a customizable ISA in a disruptively innovated manner
EdgeQ

Storage
Efficient cores to enable scalable performance for enterprise storage

Mobile

IoT MCU

AI

5G

Storage

Datacenter Cloud Solution
Vector and ACE-enabled cores for optimized AI Accelerators
Telink

Small but powerful cores for max flexibility
Picocom

Flexible interface to construct small MP for consumer storage
RISC-V Deployment – Renesas ASSP

• Renesas Selects Andes RISC-V 32-Bit CPU Cores for its First RISC-V Implementation of ASSPs

• 2020October 01
  – TOKYO, Japan — Renesas Electronics Corporation (TSE:6723), a premier supplier of advanced semiconductor solutions, today announced a technology IP cooperation with Andes Technology, an advanced supplier of RISC-V based embedded CPU cores and associated SoC development environment. Renesas selected the AndesCore™ IP 32-bit RISC-V CPU cores to embed into its new application-specific standard products that will begin customer sampling in the second half of 2021.

RISC-V Deployment - PICOCOM

- OpenRAN Family PC802
- Using 2x Andes N25F x16 clusters
  - Single issue
  - FPU (SP/DP)

RISC-V Deployment - HPMicro

- HPM6000 Family
- Based on Andes D45
  - Dual issue, 8-stage superscalar
  - FPU (SP/DP)
  - PackedSIMD/DSP extension

- Segger support
  - Free Segger IDE for user
  - Jlink supported

- OS
  - FreeRTOS
  - Zephyr
  - RT-Thread

RISC-V Deployment – Renesas GP MPU

Pioneering RZ/Five General-Purpose MPUs with 64-Bit RISC-V CPU Core

RZ/Five Block Diagram

- System
  - Debugger
  - 16ch DMAC
  - Interrupt Controller
  - PLL/SCG

- Timers
  - 1 x 32-bit MTU3
  - 8 x 16-bit MTU3
  - 1 x WDT

- Analog
  - 2 input 12-bit ADC (1 unit)
  - Thermal Sensor

CPU
- AX4MP Single (1GHz)
- With SIMO / FPU
- I-L1: 32KB, D-L1: 32KB
- TCM1/MCM: Total 12KB (1GHz)
- L2: 256KB

Internal Memory
- 512KB

Security
- Secure Boot
- Crypto Engine
- Secure JTAG
- TRNG
- OTP 1KB

Interfaces
- DDR4/DDR3L 16-bit x 1.6/1.3Gbps
- 1 x SPI Multi IO (4bit DDR)
- 2 x SDHC/USB-2/MMC
- 1 x USB2.0 Host
- 1 x USB2.0 Host / Function
- 2 x 100/1000 Ether MAC
- 4 x DC
- 2 x SCI (I/O, incl. HDA)
- 5 x SCI (UART)
- 3 x RSPI
- 4 x SSTP2
- 1 x SRC
- 2 x CAN
- GPIO

Package
- 1.1mm x 1mm BGPA
- 1.1mm x 1mm BGPA
- 2mm x 2mm BGPA
- 2mm x 2mm BGPA

RZ/Five
- Main CPU: 64-bit RISC-V x1
- Sub CPU: –
- Gigabit Ethernet: 2ch or 1ch
- CAN-FD: 2ch
- 12-bit ADC: 2ch
- Package: 1.1mm x 1mm BGPA

RZ/G2UL
- Main CPU: Cortex-A55 x1
- Sub CPU: Cortex-M33 x1
- Gigabit Ethernet: 2ch
- CAN-FD: 2ch
- 12-bit ADC: 2ch
- Package: 1.1mm x 1mm BGPA

RZ/G2LC
- Main CPU: Cortex-A55 x2 or x1
- Sub CPU: Cortex-M33 x1
- Gigabit Ethernet: 1ch
- CAN-FD: 2ch
- 12-bit ADC: 2ch
- Package: 1.1mm x 1mm BGPA

RZ/G2L
- Main CPU: Cortex-A55 x2 or x1
- Sub CPU: Cortex-M33 x1
- Gigabit Ethernet: 8ch
- CAN-FD: 2ch
- 12-bit ADC: 2ch
- Package: 2mm x 2mm BGPA

--- Pin Compatible ---
RISC-V goes BIG

- RISC-V is moving up
  - From small MCU to mid end and on the way to high end Cores

- Adoption of RISC-V is growing
  - From first AI and special use case to standard MCU’s

- How to see RISC-V goes Big?
  - More adoption in more generic use cases
  - More industrial adoption
  - Automotive adoption
Who is Andes
Andes Technology Corporation

Who We Are

- **CPU**
  - Pure-play CPU IP Vendor

- **17-year-old Public Company**
  - TPE: 6533

- **RISC-V**
  - Founding Premier Member
  - Ambassador
  - Running Task Groups
  - TSC Steering Committee Director of the Board

- **Major Open-Source Contributor/Maintainer**

Quick Facts

- **17 years in business**
  - Delivering leading CPU IP

- **250+ Licensees**

- **20K+ AndeSight IDE installations**

- **80% R&D**

- **>10B+ Total shipment of Andes-Embedded™ SoC**

Taking RISC-V® Mainstream
Andes RISC-V
Added Value and contributed extensions
Andes Added Value in RISC-V

❖ Andes extensions to RISC-V

• Baseline ISA extension to speed up memory access and branches
• CoDense to reduce code size (12% better measured by GCC)
• PowerBrake to save power by stalling pipeline
• StackSafe HW stack protection
• vPLIC vectored dispatch and preemption (reduce 57% of latency)

❖ Powerful features to differentiate your products
❖ Create competitive edge for your systems
RISC-V DSP Extension (Packed SIMD/DSP)

- Andes contributed market-proven DSP(SIMD) as P-Extension
- Designed to accelerate slow video, audio/voice and low data rate DSP workloads
- Use standard GPR for controlling
- Functions: basic, complex, controller, filtering, matrix, statistics, transform and utility functions

Real world speedup using P-Extension

<table>
<thead>
<tr>
<th>Application</th>
<th>RV32P</th>
<th>RV64P</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP3 decode</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>AMR voice codec</td>
<td></td>
<td>3.7</td>
</tr>
<tr>
<td>ML-KWS (keyword spotting)</td>
<td></td>
<td>5.2</td>
</tr>
<tr>
<td>PNET (90% of Face Detection)</td>
<td>8.9</td>
<td></td>
</tr>
<tr>
<td>CIFAR10 (Image Classification)</td>
<td>14</td>
<td>16</td>
</tr>
</tbody>
</table>

Speed Up (times)
Andes Custom Extension – EDA Tool

- ACE unlocks RISC-V’s Potential of RISC-V DSA
  - Define ACE instructions to handle time critical codes
  - Another approach to co-processor or accelerators

- All-in-one COPILOT development environment
  - EDA Automation tool and ease of use
  - Extensions are easy to re-use, can be used as a library
Andes RISC-V and ISO26262

- ISO26262 qualification achieved (Andes certified by December 2020 up to ASIL-D)

- ASIL-B development of N25F
  - Expect Engineering Version Ready
  - Certified by SGS/TUV by Q2, 2021

- More Cores to come, contact Andes
Andes RISC-V Roadmap
AndesCore™ RISC-V Processor Lineup

1. Core naming: with "X" is 64-bit (e.g. NX25F) and no "X" is 32-bit (e.g. N25F).
2. V5's common features include RV-IMACN, Caches, LM, ECC/parity, Branch Prediction, CoDense™, PowerBrake, StackSafe™, ACE (Andes Custom Extension™); Frequencies is the worst case at 28nm.

*: TSMC 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.

Taking RISC-V® Mainstream
Andes 45-Series CPU Cores
45-Series: Features

- AndeStar™ V5 architecture:
  - Base: RV*GCN + Andes V5 extensions
  - N45/NX45: base
  - D45: base + P
  - A45/AX45: base + P + MMU
  - A45MP/AX45MP: base + P + MMU

- 8-stage in-order dual-issue
  - Independent pairs with 1 or 2 ALU insns
  - Most dependent pairs with 2 ALU insns
  - Late ALU for 0-cycle load-use penalty

- Unaligned data accesses

- Low power dynamic branch prediction

- MemBoost memory subsystem
A(X)45MP: Cache-Coherent Multicore

- **Cache coherence scheme**
  - Directory-based for scalability
  - MESI coherence protocol
- **45MP Coherence Manager**
  - Support 1~4 A45/AX45
  - IO coherence for cacheless masters
- **L2$ Controller** (optional)
  - Up to 2MB, 2 tag&data
- **Bus Interfaces**
  - Memory and MMIO ports
  - LM slave ports (one per core)
  - Coherence slave port
- **PLIC** for global interrupt handling
- **Debug/trace** support
- **Linux SMP** ready

AndesCore™
A*45MP Multicore

- Platform-Level Interrupt Controller
- Debug Support
- Coherence Manager
- L2 Cache Controller

- IRQ’s
- JTAG
- Trace Ports
- LM Slave Ports (AXI)
- Coherence Slave Port (AXI-128)
- MMIO (AXI-128) to Memory (AXI-128)
AE350 Pre-integrated Platforms

Taking RISC-V® Mainstream
Andes RISC-V Vector Processor
NX27V: Overview

- 5-Stage scalar with VPU
  - Latest RV-V specification
- RVV data formats:
  - Standard: int8~int64, fp16~fp64
  - Andes-extended: bfloat16 and int4
- A powerful Vector Unit (VPU):
  - RVV starts execution after retired
  - Multiple Functional Units
    - Operating in parallel and out of order
    - Chainable, and most fully pipelined
  - VLEN & SIMD width: 128, 256, 512
- Independent memory access paths:
  - RVV load/store thru dcache and system bus
  - ACE load/store thru Streaming Port
Andes RISC-V environment
SoC SW Development Environment

**AndeSight™ IDE**
- Eclipse-Based IDE
- Streamlined GUI
- Feature-rich Editor
- Managed Build System
- Optimized Toolchains
- Source Level Debugger
- Profiling Analysis
- Extensive Demo Projects
- Flash ISP

**AndeSoft™ SW Stack**
- Application Layers
- Middleware
- Drivers
- App Drivers
- OS/Kernel
- Libraries

**Virtual SoC**
- Virtual SoC Configuration
- Profiling/Tracing/Debugging data

**Andes/Partners’ Solutions**
- Andes/Partners’ Solutions
- Customers’ Designs

**AndeShape™**
- AndeShape™
- AndesCore™ Bus Controller
- 10/100 MAC
- USB2.0
- LCD Controller
- SDRAM Controller
- DMA Controller
- SRAM Controller
- PWM
- I2C GPIO INT
- WDT Timer RTC
- ST UART
- BT UART
- SSP CF
- I²S SD/MMC
- Power Manager
- AHB to APB Bridge
- AHB Bus
- APB Bus

**Taking RISC-V® Mainstream**
Andes Partners and Ecosystem

AI tools, SW and IP
- Deeplite
- PEAKHILLS
- Keron
- easics
- tvm
- ONNC
- TensorFlow
- ELVM
- OpenCL
- multicoreware
- D2 technologies
- m-center
- UNILAB
- OPEN AI LAB
- RELA JET
- sensory

DSP, Audio and Vision
- Cyberon
- UnlimitKear
- OPEN AI LAB
- RELA JET
- sensory

Development tools
- SEGGER
- imperas
- IAR Systems
- LAUTERBACH
- ultra soc

Security
- Rambus
- ememory
- verimatrix
- Virtual Open Systems
- INTRINSIC ID
- SECURE-IC
- Veridify Security
- 0x5
- Tiempo
- wolfSSL
- Dovere Microsystems
- HEX-Flow
- SILEX INSIGHT
- THREADX

RTOS
- newt
- RT-Thread
- RTEMS
- uC3
- uC/OS
- RTOS technologies
- AliOS Things
- SylinxOS
- RT-Thread
- Zephyr

Taking RISC-V® Mainstream
Andes Wrap up

- **Andes Technology : your Trusted Partner!**
  - Over 10 Billion Cores shipped
  - 17 year old, Public Company
  - ISO26262 up to ASIL-D certified

- **Lineup of Andes V5 RISC-V Processors**
  - From small power saving MCU up to powerful Vector units
  - From single Core to MultiProcessor with L1 Cache/IO coherence and L2 Cache

- **RISC-V goes BIG**
  - Be sure to be future ready, add RISC-V now, talk to Andes
Thank you

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