ANDES TECHNOLOGY

Spring 2022 RISC-V Week Paris

RISC-V®

Tuesday 3rd to Thursday 5th May 2022

RISC-V goes BIG

Florian Wohlrab

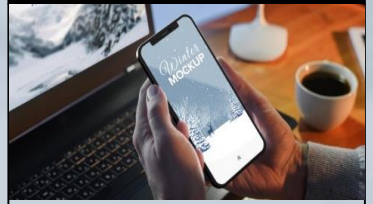
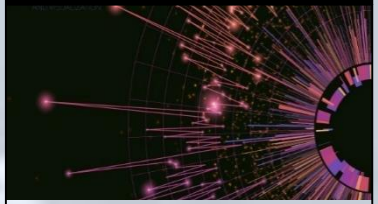
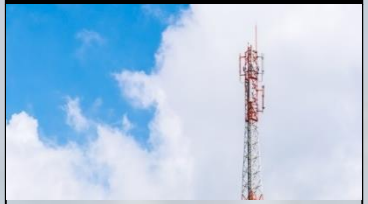
Sales Manager EMEA & Japan,
Andes Technology

2022/May/05

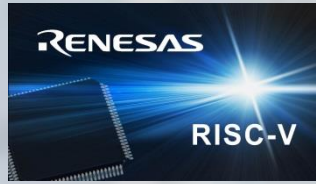
Agenda

- Why RISC-V goes BIG
- Who is Andes
- Andes RISC-V Core Features
- Andes RISC-V Roadmap
- Andes RISC-V enviroment

RISC-V Powering Industry Leaders

Mobile	IoT MCU	AI	5G	Storage
				
Mobile AP **TDDI** Billions shipment of connectivity, touch, and sensor hub.	RENESAS Performance, safety and customization enabling innovative ASSP MCU Telink Serving mainstream audio, wearables and IoT development needs	SK telecom Configurable and efficient core to power high-performance AI **Datacenter Cloud Solution** Vector and ACE-enabled cores for optimized AI Accelerators	EDGEQ 5G WITH AN EDGE a customizable ISA in a disruptively innovated manner picocom Empowering Wireless Small but powerful cores for max flexibility	Efficient cores to enable scalable performance for enterprise storage  Flexible interface to construct small MP for consumer storage

RISC-V Deployment – Renesas ASSP



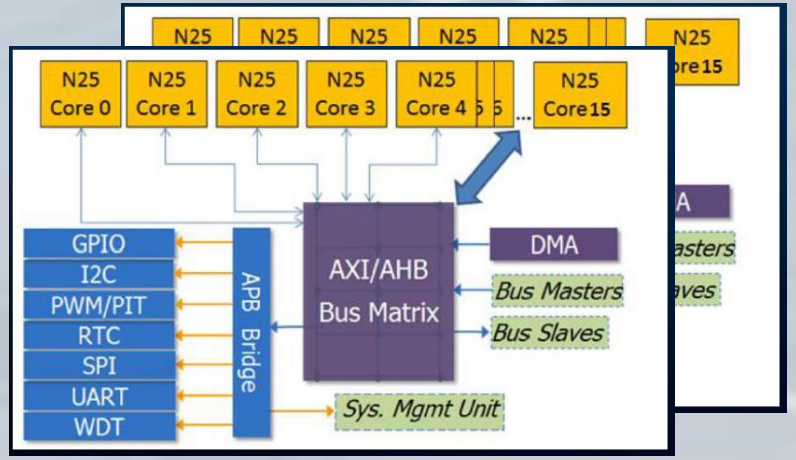
- Renesas Selects Andes RISC-V 32-Bit CPU Cores for its First RISC-V Implementation of ASSPs

- 2020October 01
  - TOKYO, Japan — **Renesas Electronics Corporation** (TSE:6723), a premier supplier of advanced semiconductor solutions, today announced a technology IP cooperation with **Andes Technology**, an advanced supplier of RISC-V based embedded CPU cores and associated SoC development environment. Renesas selected the AndesCore™ IP **32-bit RISC-V CPU cores** to embed into its new **application-specific standard products** that will begin customer sampling in the second half of 2021.

- **https://www.renesas.com/eu/en/about/press-center/news/2020/news20201001.html**

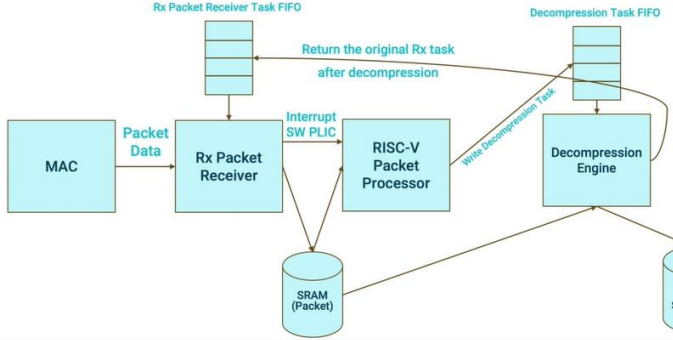
RISC-V Deployment - PICOCOM

- OpenRAN Family PC802
- Using 2x Andes N25F x16 clusters
  - Single issue
  - FPU (SP/DP)



PicoCom's PC802 12nm chip has 32 RISC-V cores and four have been designed to an OpenRAN control board called ORANIC

Recycling Descriptors



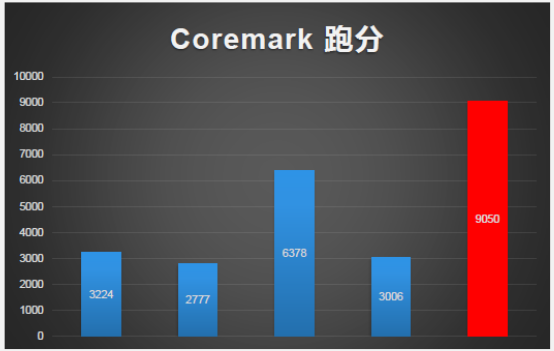
https://picocom.com/picocom-high-performance-soft-packet-processing-features-at-andes-technology-risc-v-con-virtual-2021/

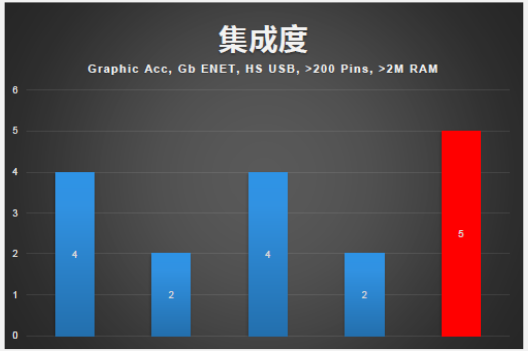
RISC-V Deployment - HPMicro

- HPM6000 Family
- Based on Andes D45
  - Dual issue, 8-stage superscalar
  - FPU (SP/DP
  - PackedSIMD/DSP extension
- Segger support
  - Free Segger IDE for user
  - Jlink supported
- OS
  - FreeRTOS
  - Zephyr
  - RT-Thread

国际高端MCU比较表

	国际品牌 MCU1	国际品牌 MCU2	国际品牌 MCU3	国际品牌 MCU4	HPM6750
CPU	ARM Cortex-M7/M4	ARM Cortex-M7	ARM Cortex-M7/M4	ARM Cortex-M7	RISC-V X 2
主频	480 MHz	550 MHz	1 GHz	600 MHz	800 MHz





High Performance RISC-V General Purpose MCU
基于创新架构的高性能RISC-V 通用MCU

https://www.eet-china.com/news/202112172147.html

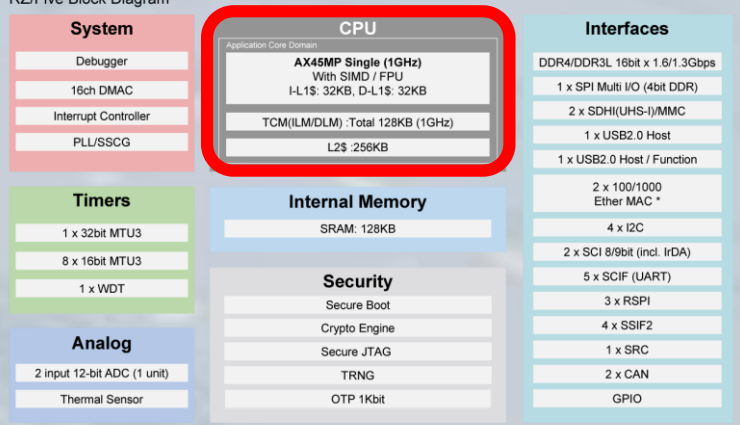
RISC-V Deployment – Renesas GP MPU

	NEW RZ/Five	RZ/G2UL	RZ/G2LC	RZ/G2L
Main CPU	64-bit RISC-V x1	Cortex-A55 x1	Cortex-A55 x2 or x1	Cortex-A55 x2 or x1
Sub CPU	–	Cortex-M33 x1	Cortex-M33 x1	Cortex-M33 x1
Gigabit Ethernet	2ch or 1ch	2ch	1ch	2ch
CAN-FD	2ch	2ch	2ch	2ch
12-bit ADC	2ch	2ch	–	8ch
Package	13mm Square BGA * 11mm Square BGA	13mm Square BGA *	13mm Square BGA	15mm Square BGA 21mm Square BGA

* Pin Compatible

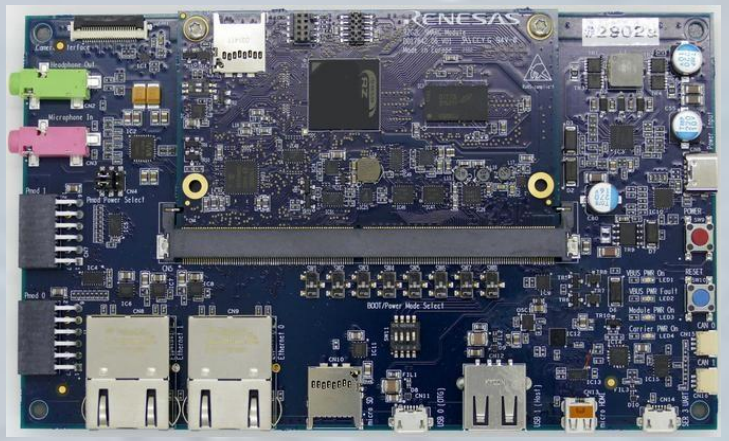
RENESAS

RZ/Five Block Diagram



* : The 266pin package has one channel of Gigabit Ethernet.

Package Information : 361pin, 13x13mm PBGA (0.5mmPitch)
266pin, 11x11mm PBGA (0.5mmPitch)



RISC-V goes BIG

- RISC-V is moving up
  - From small MCU to mid end and on the way to high end Cores
- Adoption of RISC-V is growing
  - From first AI and special use case to standard MCU's
- How to see RISC-V goes Big?
  - More adoption in more generic use cases
  - More industrial adoption
  - Automotive adoption

Who is Andes

Andes Technology Corporation

Who We Are

Pure-play
CPU IP Vendor

RISC-V Founding
Premier Member

Major Open-Source
Contributor/Maintainer

17-year-old
Public Company
TPE: 6533

RISC-V Ambassador
Running Task Groups
TSC Steering Committee
Director of the Board

Quick Facts

17 years in business
Delivering leading CPU IP

80%
R&D

250+
Licensees

20K+
AndeSight IDE installations

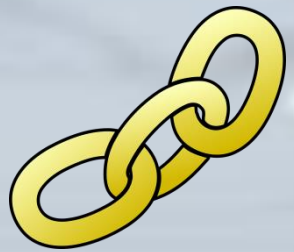
>10B+
Total shipment of Andes-Embedded™ SoC

Andes RISC-V

Added Value and contributed extensions

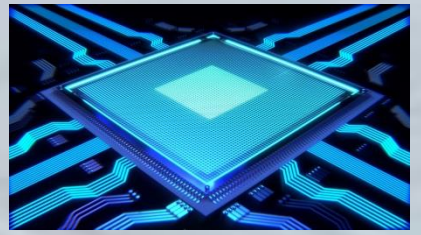
Andes Added Value in RISC-V

- Andes extensions to RISC-V

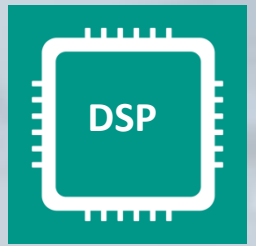


  - Baseline ISA extension to speed up memory access and branches
  - CoDense to reduce code size (12% better measured by GCC)
  - PowerBrake to save power by stalling pipeline
  - StackSafe HW stack protection
  - vPLIC vectored dispatch and preemption(reduce 57% of latency)

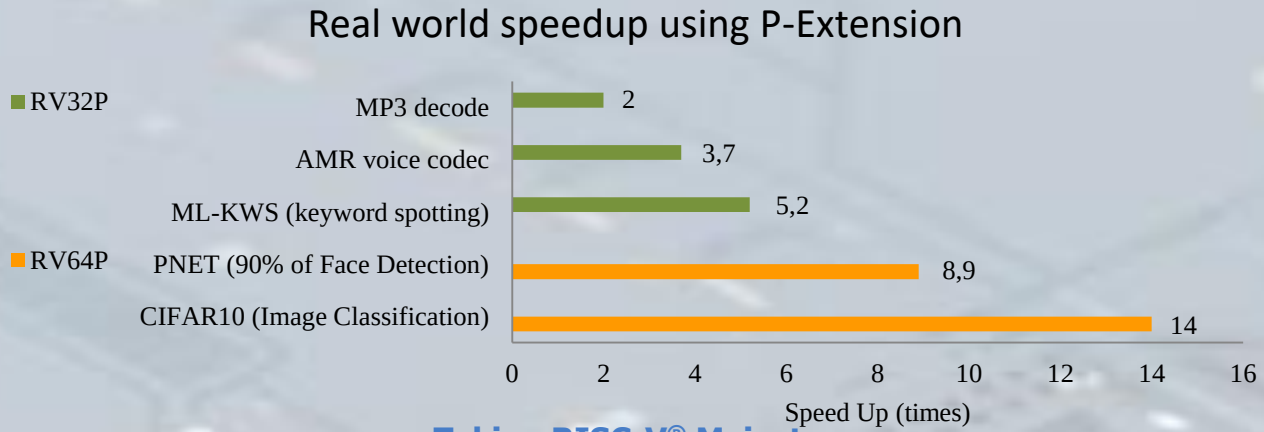
- Powerful features to differentiate your products
- Create competitive edge for your systems



RISC-V DSP Extension (Packed SIMD/DSP)



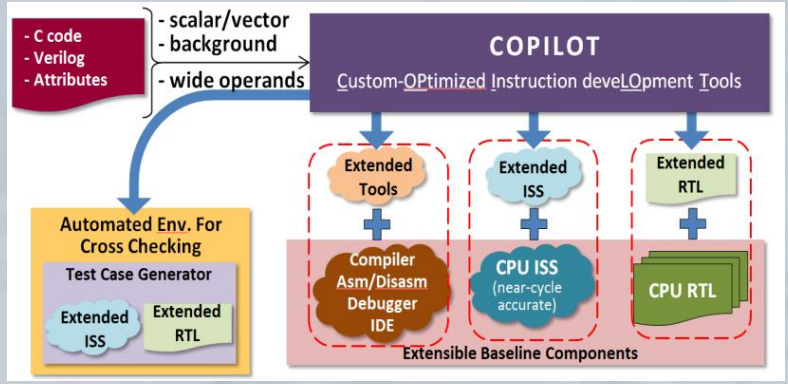
- Andes contributed market-proven DSP(SIMD) as P-Extension
- Designed to accelerate slow video, audio/voice and low data rate DSP workloads
- Use standard GPR for controlling
- Functions: basic, complex, controller, filtering, matrix, statistics, transform and utility functions



Andes Custom Extension – EDA Tool

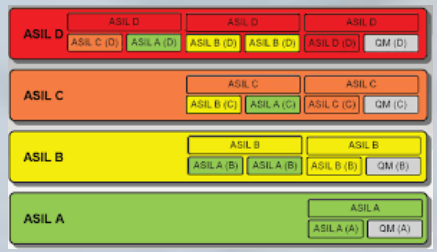
- ACE unlocks RISC-V's Potential of RISC-V DSA
  - Define ACE instructions to handle time critical codes
  - Another approach to co-processor or accelerators

- All-in-one **COPILOT** development environment
  - EDA Automation tool and ease of use
  - Extensions are easy to re-use, can be used as a library



Andes RISC-V and ISO26262

- ISO26262 qualification achieved
  (Andes certified by December 2020 up to ASIL-D)



ISO 26262
Road Vehicles - Fuctional Safety

- ASIL-B development of N25F
  - Expect Engineering Version Ready
  - Certified by SGS/TUV by Q2,2021

- More Cores to come, contact Andes

SGS TÜV SAAR

CERTIFICATE NO.: FS/71/220/20/0639 PAGE 1/1

LICENCE HOLDER

ANDES TECHNOLOGY CORPORATION
10F., NO. 1, SEC. 3, GONGDAO 5TH RD., EAST DIST.,
HSINCHU CITY
TAIWAN R.O.C 30069

Project-No/-ID	LICENSED TEST MARK	Report No.
P30L	SGS TÜV SAAR FUNCTIONAL SAFETY APPROVED	P30L0001

Tested according to: ISO 26262:2018

Certified Process: Development process for Functional Safety related components up to ASIL D
Version V1.0/202011

Technical Data/Parameter: The audited development process complies with the ISO 26262 standard part requirements

ISO 26262-2:2018 ISO 26262-6:2018
ISO 26262-4:2018 ISO 26262-8:2018
ISO 26262-5:2018 ISO 26262-9:2018

Specific Requirements: The certificate is created for the purpose of providing conformity of the development and support process in accordance with ISO 26262. Changes which are not covered in the Audit Report have to be reconsidered.

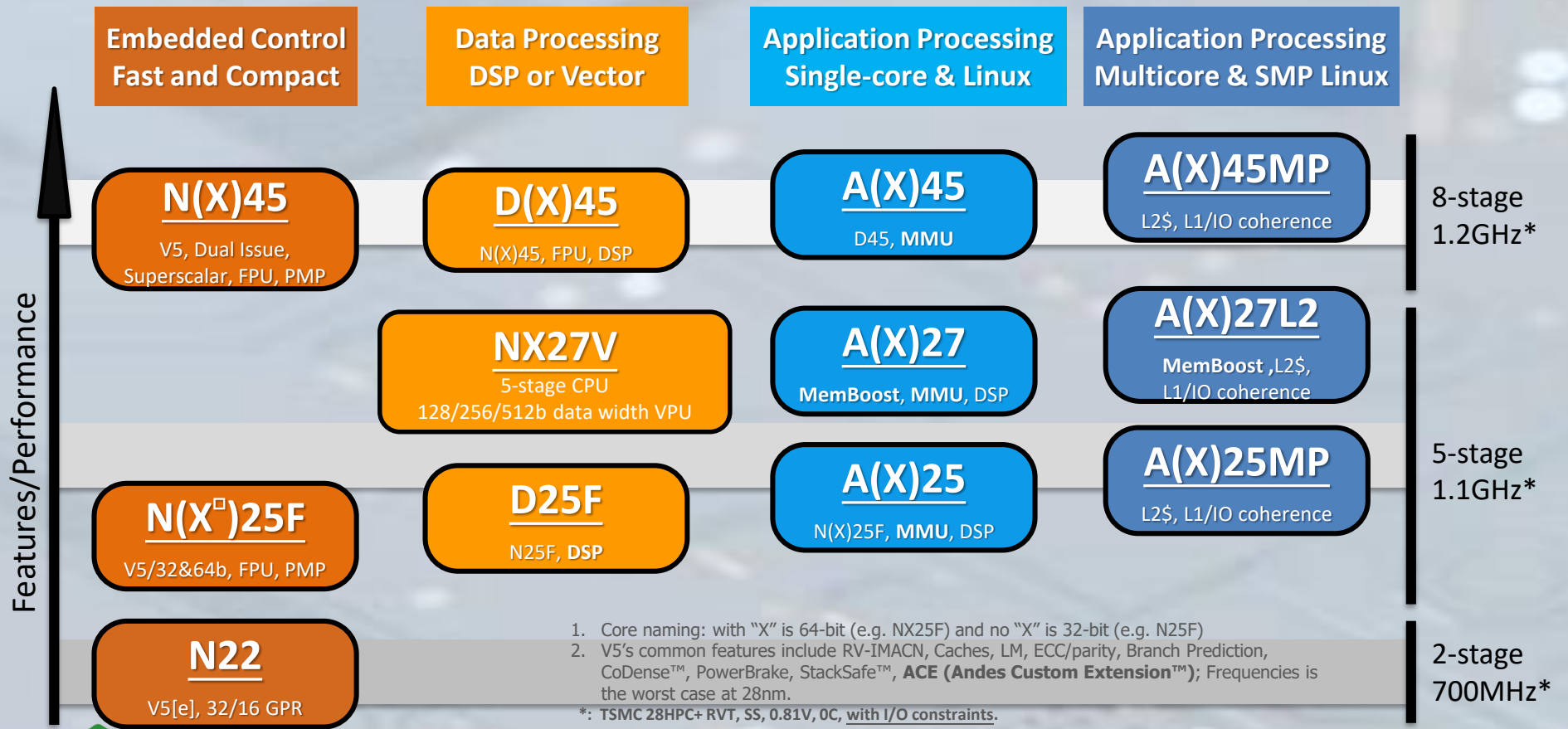
Certification Body for Functional Safety SGS-TÜV Saar GmbH

Munich, December 22nd, 2020

Marcus Rau

Andes RISC-V Roadmap

AndesCore™ RISC-V Processor Lineup



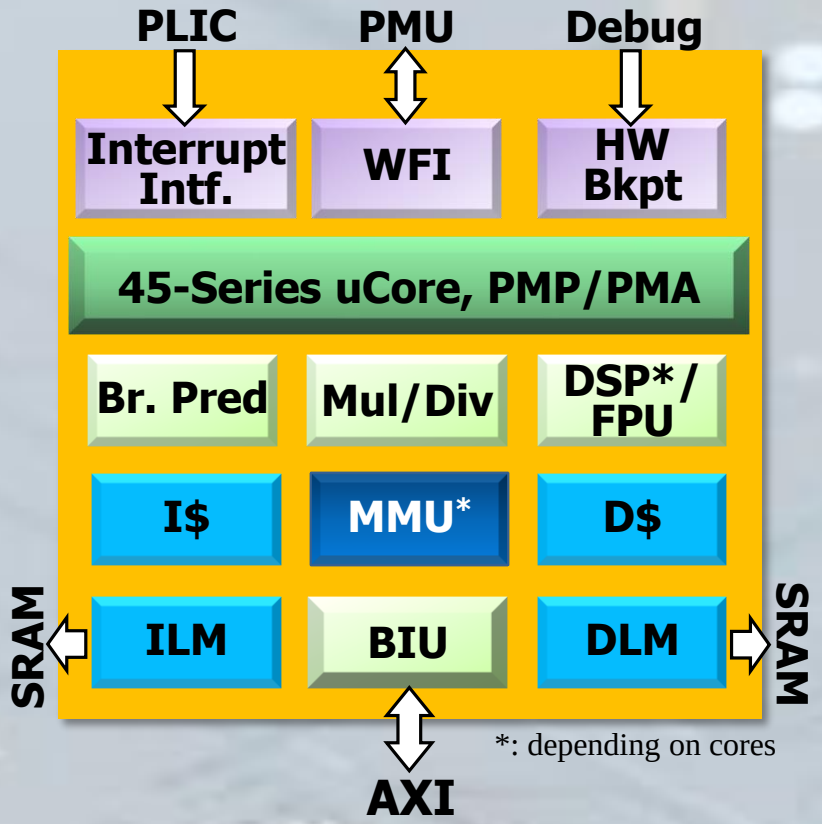
1. Core naming: with "X" is 64-bit (e.g. NX25F) and no "X" is 32-bit (e.g. N25F)
2. V5's common features include RV-IMACN, Caches, LM, ECC/parity, Branch Prediction, CoDense™, PowerBrake, StackSafe™, **ACE (Andes Custom Extension™)**; Frequencies is the worst case at 28nm.

*: **TSMC 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.**

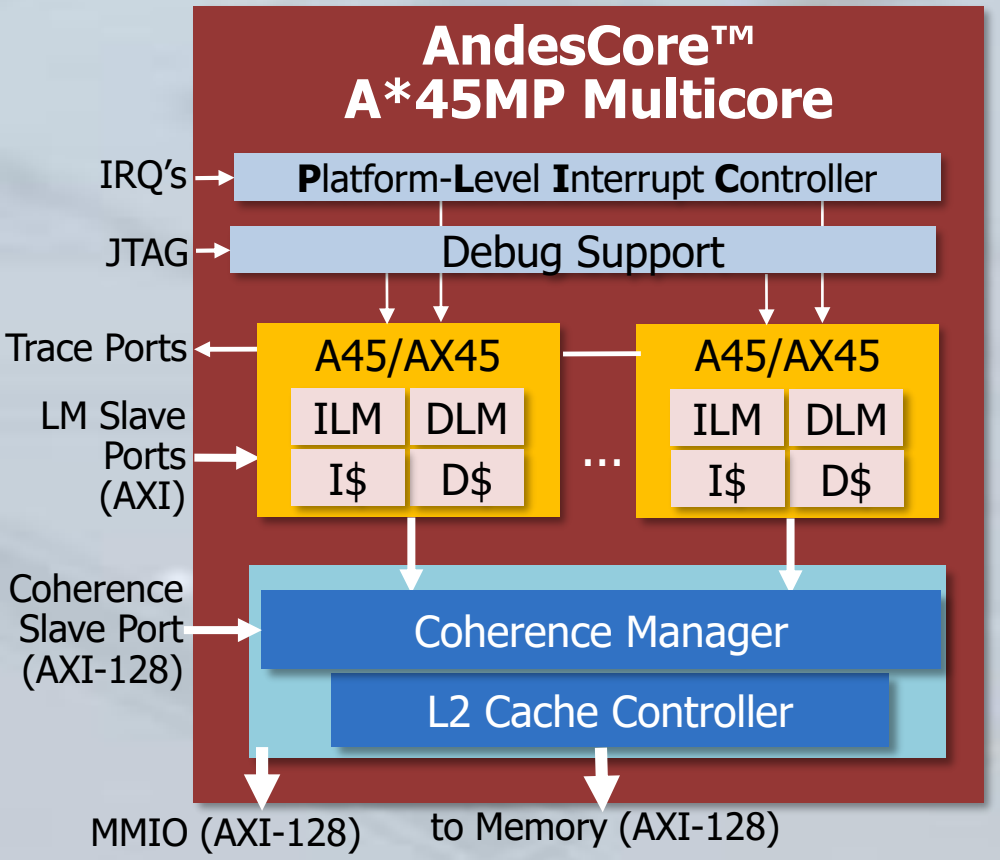
Andes 45-Series CPU Cores

45-Series: Features

- AndeStar™ V5 architecture:
  - Base: RV*GCN + Andes V5 extensions
  - N45/NX45: base
  - D45: base + P
  - A45/AX45: base + P + MMU
  - **A45MP/AX45MP**: base + P + MMU
- 8-stage in-order dual-issue
  - Independent pairs with 1 or 2 ALU insns
  - Most dependent pairs with 2 ALU insns
  - Late ALU for 0-cycle load-use penalty
- Unaligned data accesses
- Low power dynamic branch prediction
- **MemBoost** memory subsystem

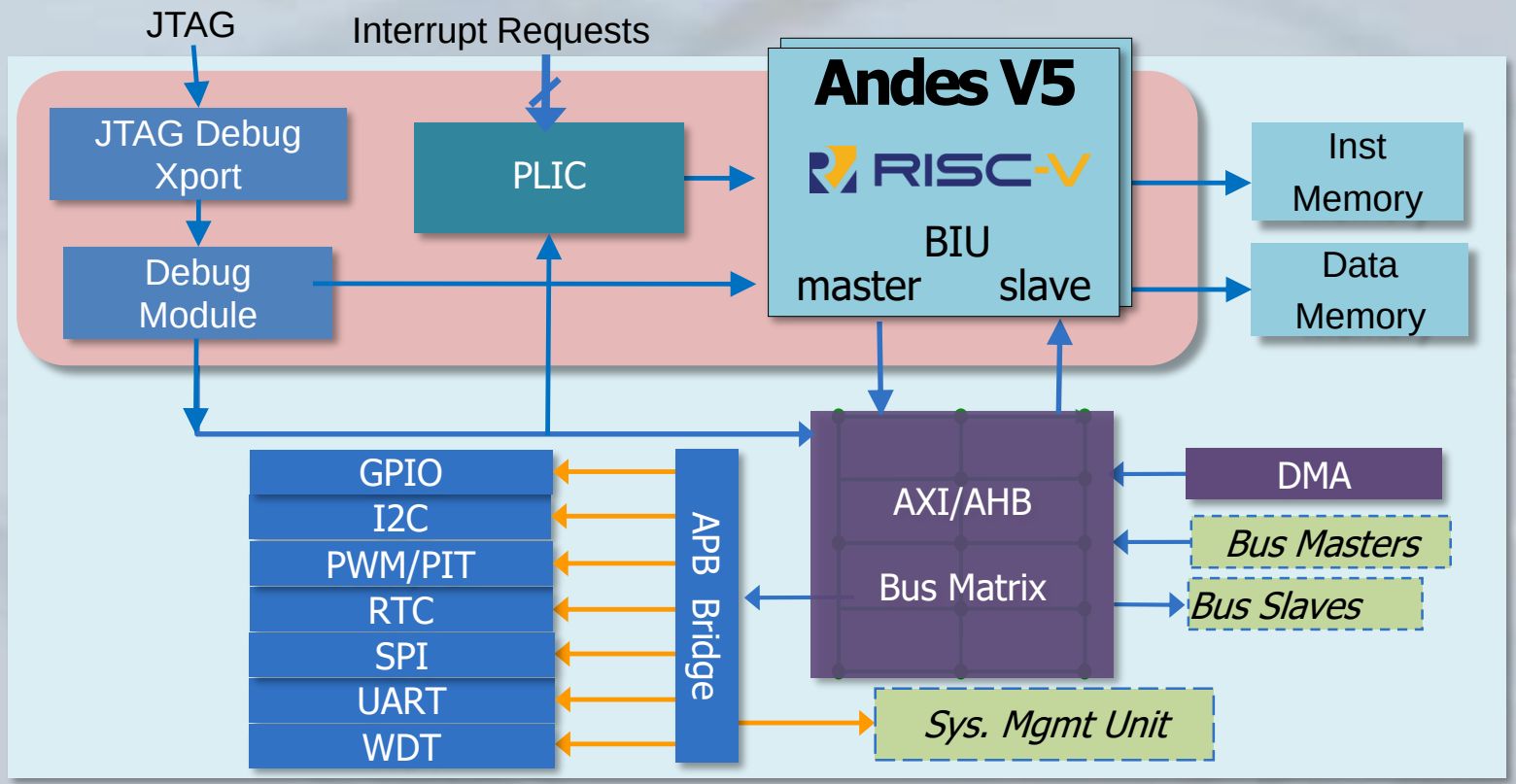


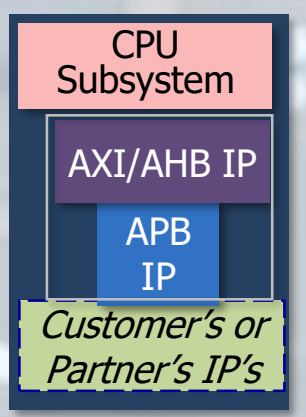
A(X)45MP: Cache-Coherent Multicore



- **Cache coherence scheme**
  - Directory-based for scalability
  - MESI coherence protocol
- **45MP Coherence Manager**
  - Support 1~4 A45/AX45
  - IO coherence for cacheless masters
- **L2$ Controller** (optional)
  - Up to 2MB, 2 tag&data
- **Bus Interfaces**
  - Memory and MMIO ports
  - LM slave ports (one per core)
  - Coherence slave port
- **PLIC** for global interrupt handling
- **Debug/trace** support
- **Linux SMP** ready

AE350 Pre-integrated Platforms

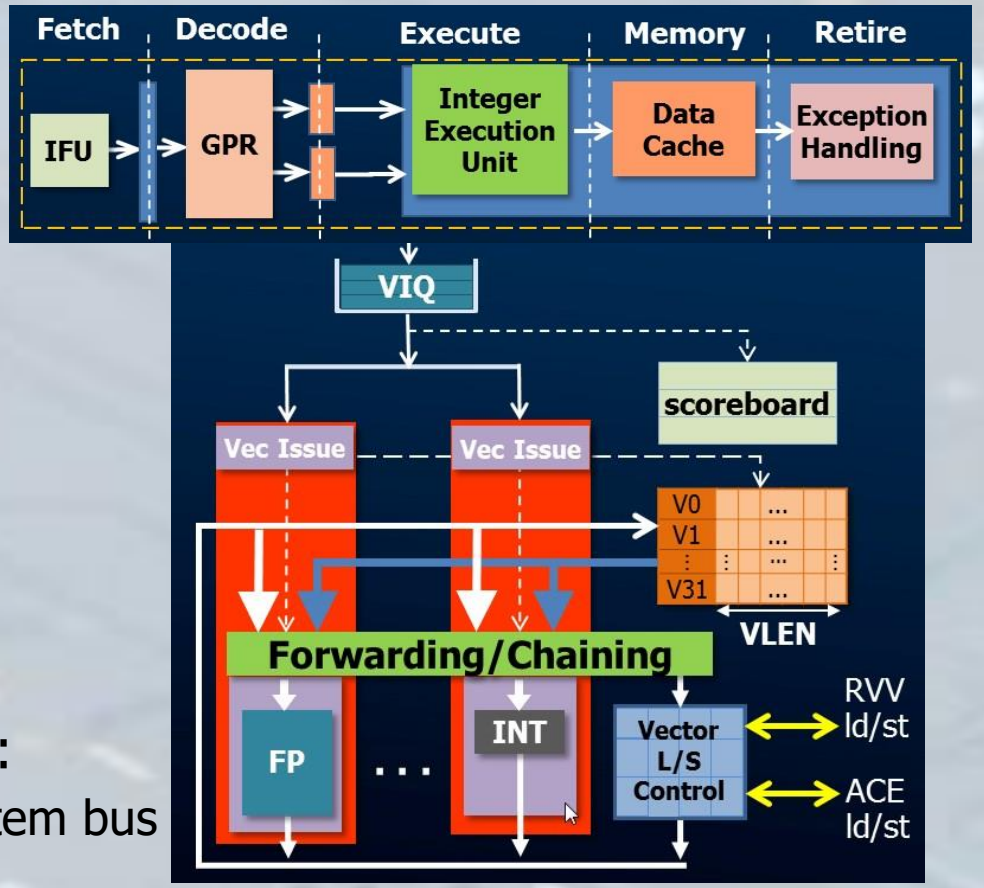




Andes RISC-V Vector Processor

NX27V: Overview

- 5-Stage scalar with VPU
  - Latest RV-V specification
- RVV data formats:
  - Standard: int8~int64, fp16~fp64
  - Andes-extended: bfloat16 and int4
- A powerful Vector Unit (VPU):
  - RVV starts execution after retired
  - Multiple Functional Units
    - Operating in parallel and out of order
    - Chainable, and most fully pipelined
  - VLEN & SIMD width: 128, 256, 512
- Independent memory access paths:
  - RVV load/store thru dcache and system bus
  - ACE load/store thru Streaming Port



Andes RISC-V environment

SoC SW Development Environment

AndeSight™ IDE

- Eclipse-Based IDE
- Streamlined GUI
- Feature-rich Editor
- Managed Build System
- Optimized Toolchains
- Source Level Debugger
- Profiling Analysis
- Extensive Demo Projects
- Flash ISP

build executables

debug interactively

AndeSoft™ SW Stack

- Application Layers
- Middleware
- Drivers | App Drivers
- OS/Kernel | Libraries

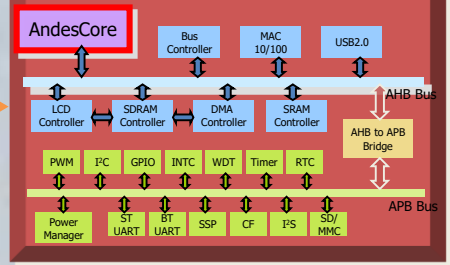
Andes/Partners' Solutions

Customers' Designs

Virtual SoC Configuration

SoC based on AndesCore™

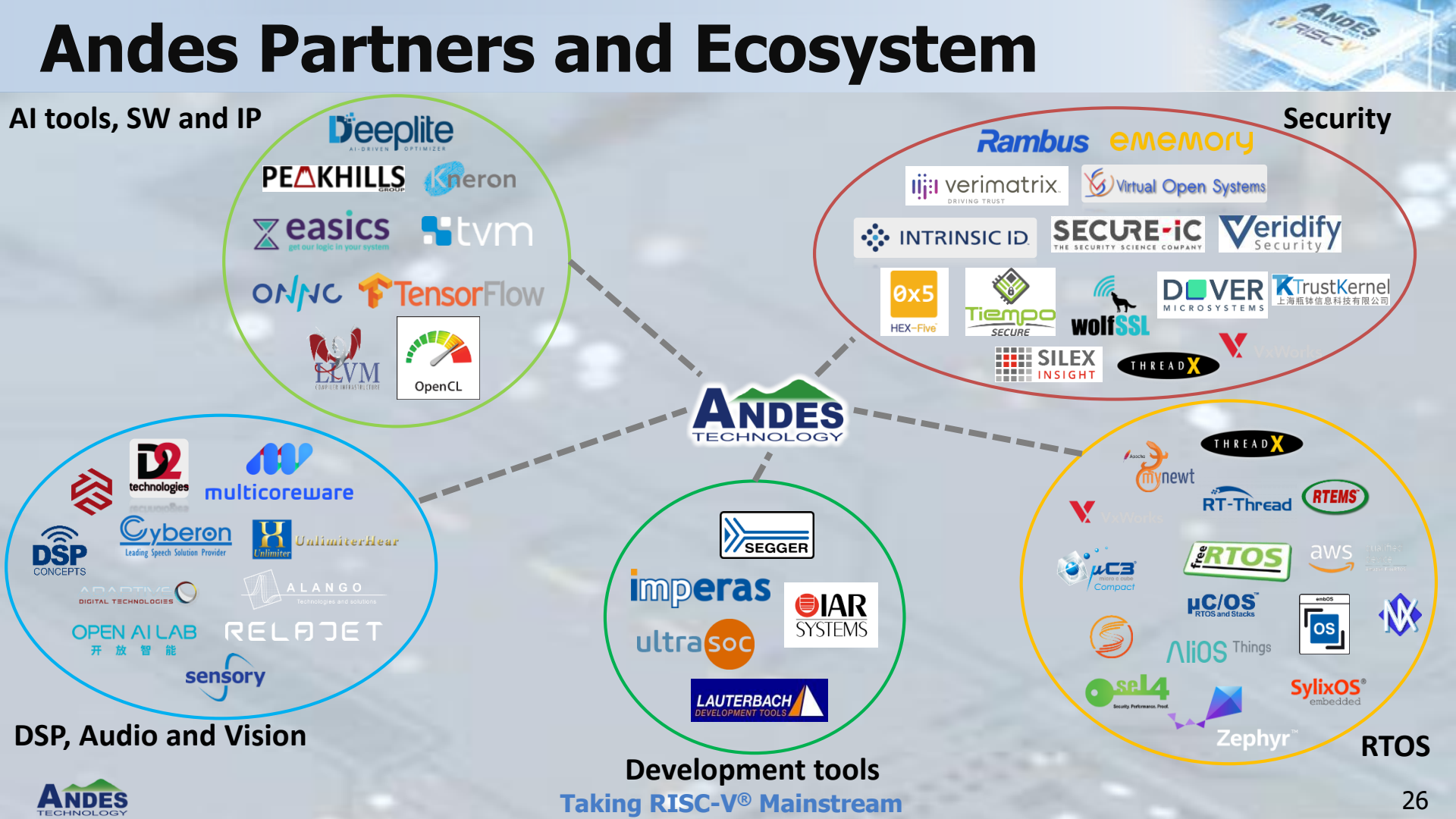
Virtual SoC



AndeShape™

Profiling/Tracing/Debugging data

Andes Partners and Ecosystem



Taking RISC-V® Mainstream

Andes Wrap up

- **Andes Technology : your Trusted Partner!**
  - Over 10 Billion Cores shipped
  - 17 year old, Public Company
  - ISO26262 up to ASIL-D certified

- **Lineup of Andes V5 RISC-V Processors**
  - From small power saving MCU up to powerful Vector units
  - From single Core to MultiProcessor with L1 Cache/IO coherence and L2 Cache

- **RISC-V goes BIG**
  - **Be sure to be future ready, add RISC-V now, talk to Andes**

florian@andestech.com

Thank you

ANDES TECHNOLOGY

florian@andestech.com