Securing the Future of Open Source Computing

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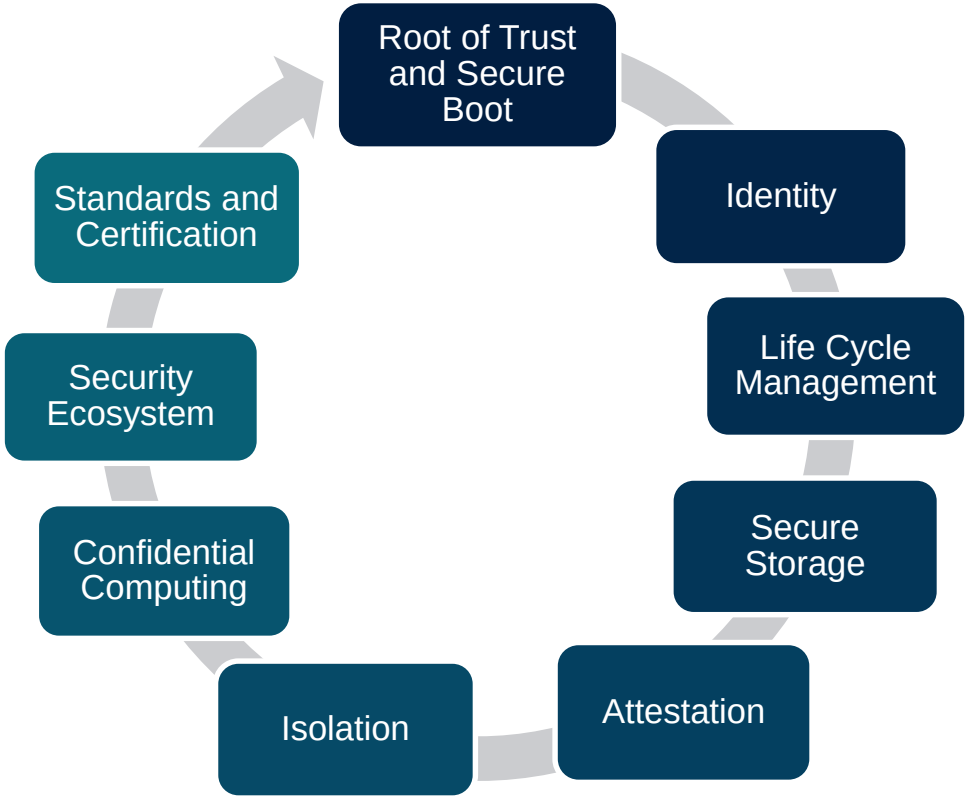
Intrinsic Security

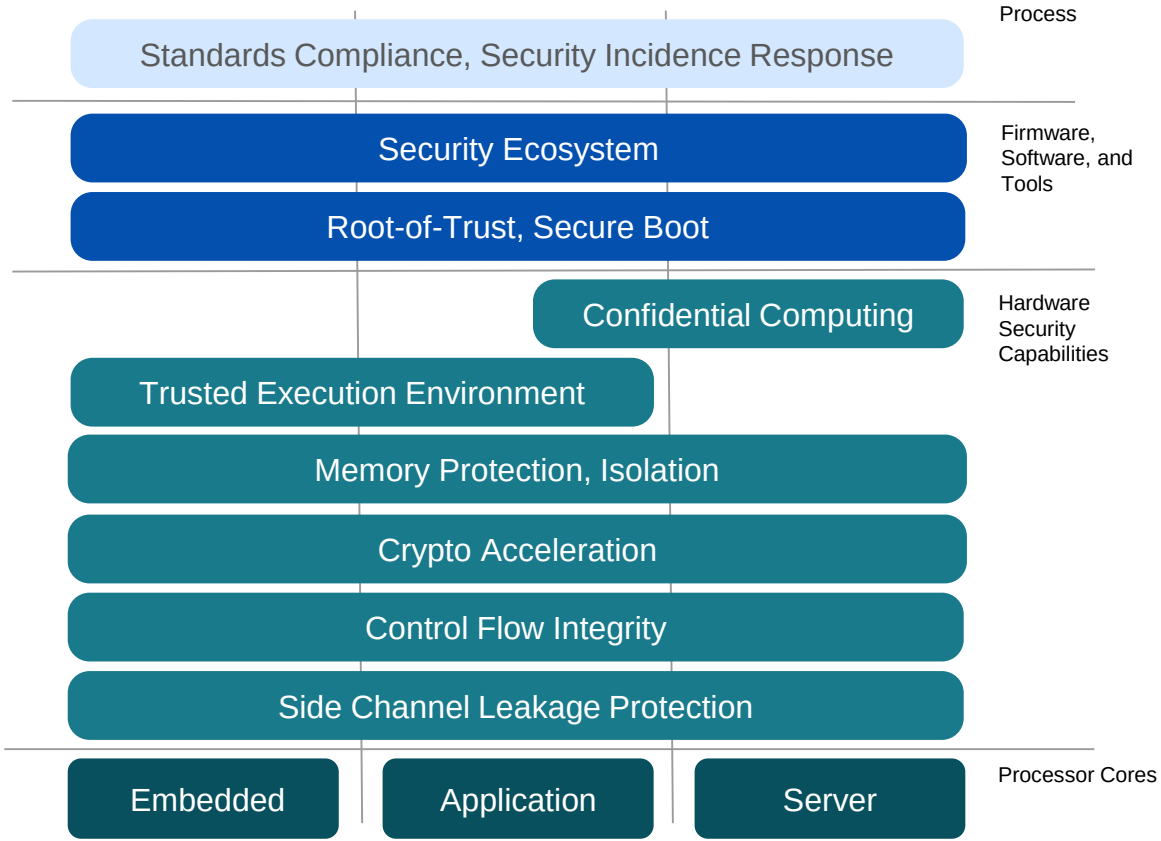
- Security as a basic feature of HW, SW Firmware
- Support security through entire lifecycle
- Published Guidelines matched to usage profiles



RISC-V Security Rationale

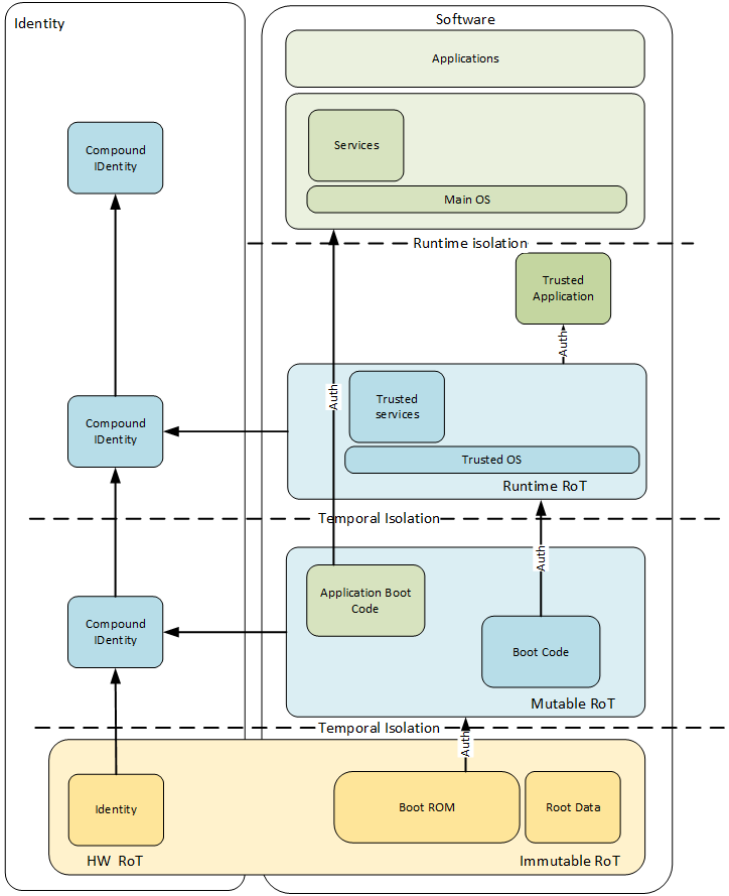
- Clean-slate architecture invites new hardware security solutions
- Open security model accelerates hardware security innovation
- Opportunity to incorporate security industry learnings & best practices
- Open governance facilitates collaboration on best security approach
- Royalty free model enables new open-source hardware security solutions

Security Scope



Security Model

- State Goals & Rationale for RISC-V Security
- Defines Scope
- Defines Threat Model
- Derives Security Requirements



Generic Device Model

Security Ecosystem

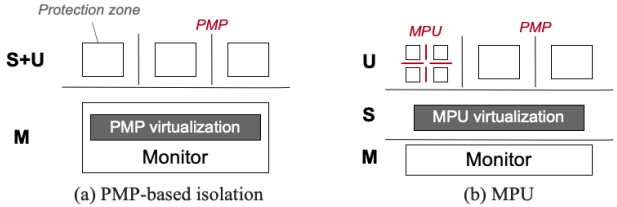
- Enablement of RISC-V security services & software
- Identify and list key open-source security software and libraries
- Develop RISC-V security reference implementation(s)
- Identify, monitor, and influence applicable standards
- Identify and liaison with applicable Security Certification entities

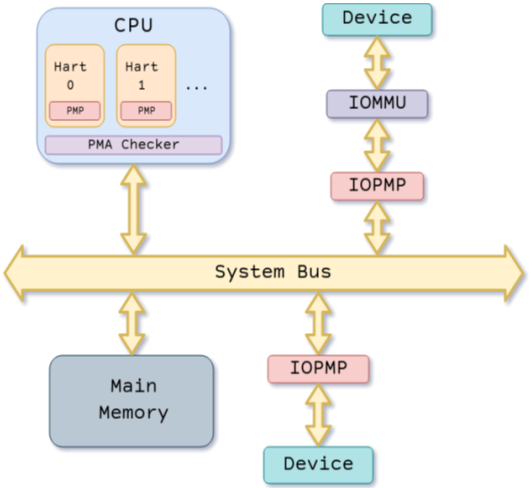
Memory Safety

- PMP
  - Basic isolation between M-mode and S/U-modes.
- ePMP
  - Enhanced PMP for increased executable protection, additional use cases
- Virtual Memory
  - Isolation between S and U mode
  - Guest-Guest Isolation (VS-VS)
  - Host –Guest Isolation (HS-VS)

under development:

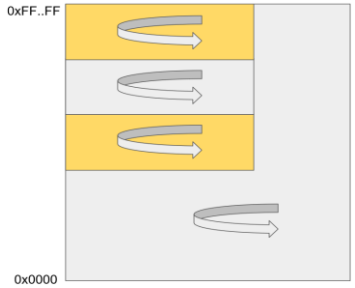
- MPU
  - Similar to S-mode PMP
- IOPMP
  - System Level PMP
  - Protects memory from other masters





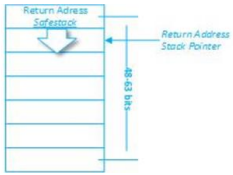
Robustness

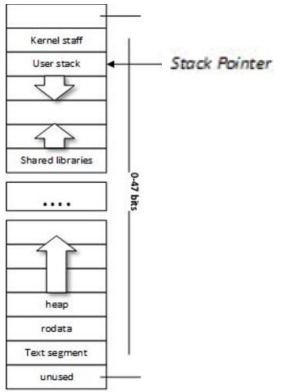
- Pointer Masking
  - actual_address = (requested_address & ~mpmmask) | mpmbase
  - Software based memory tagging
  - Memory bounding



under development:

- Control Flow Integrity
  - Shadow Stack
  - Labelled Landing Pad





- MicroArchitectural Side Channel Leakage
  - An anomaly
  - Speculation Barriers – fence.t

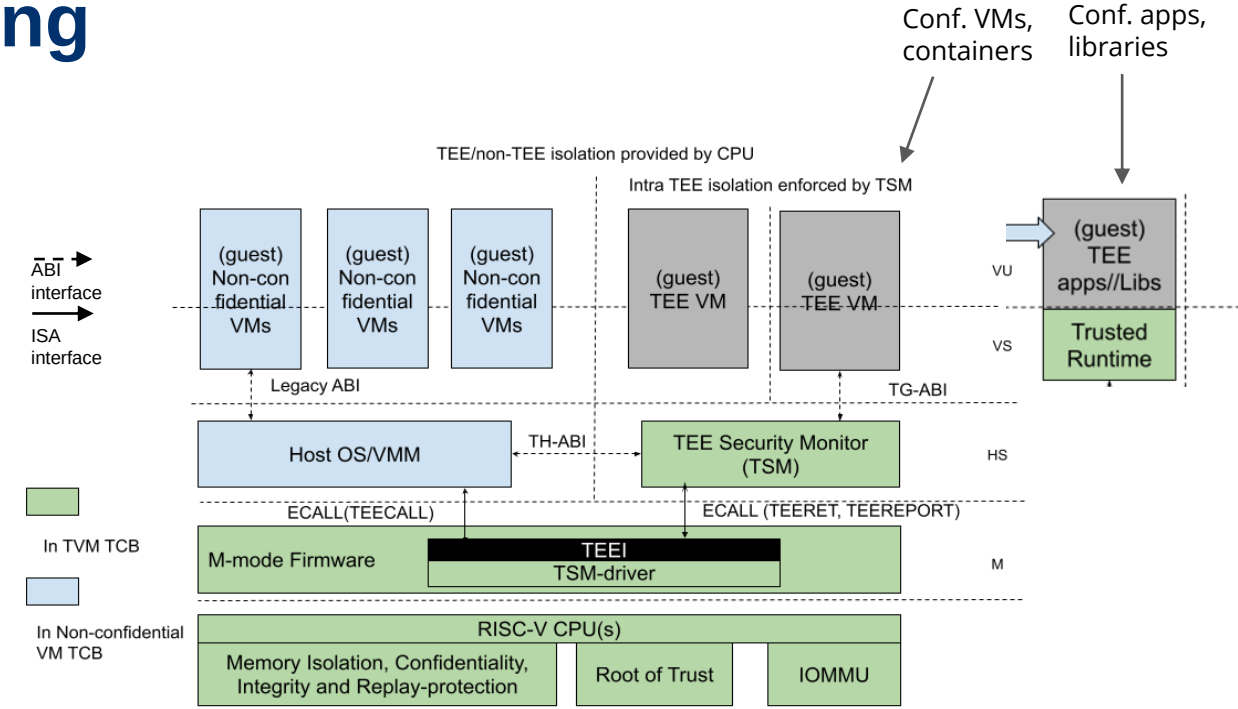
Cryptography

- Scalar Extension Ratified
- Vector Extension – 2022
- Post Quantum – under discussion

Trusted Computing

Under Development:

- Trusted Execution Environment
- APT TEE i/f to allow support on current ratified ISA
- Extensions possible to improve performance, security etc

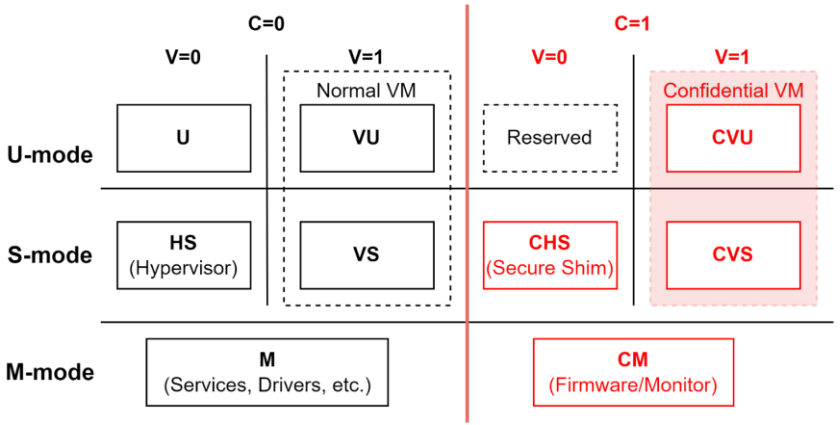


Maybe ISA affecting / **ISA Affecting**

Trusted Computing (2)

Under Development:

- Confidential Computing
  - Confidential VMs
- Extension of APP TEE
- Incorporate attestation standards



Future Potential

Requirement Under discussion

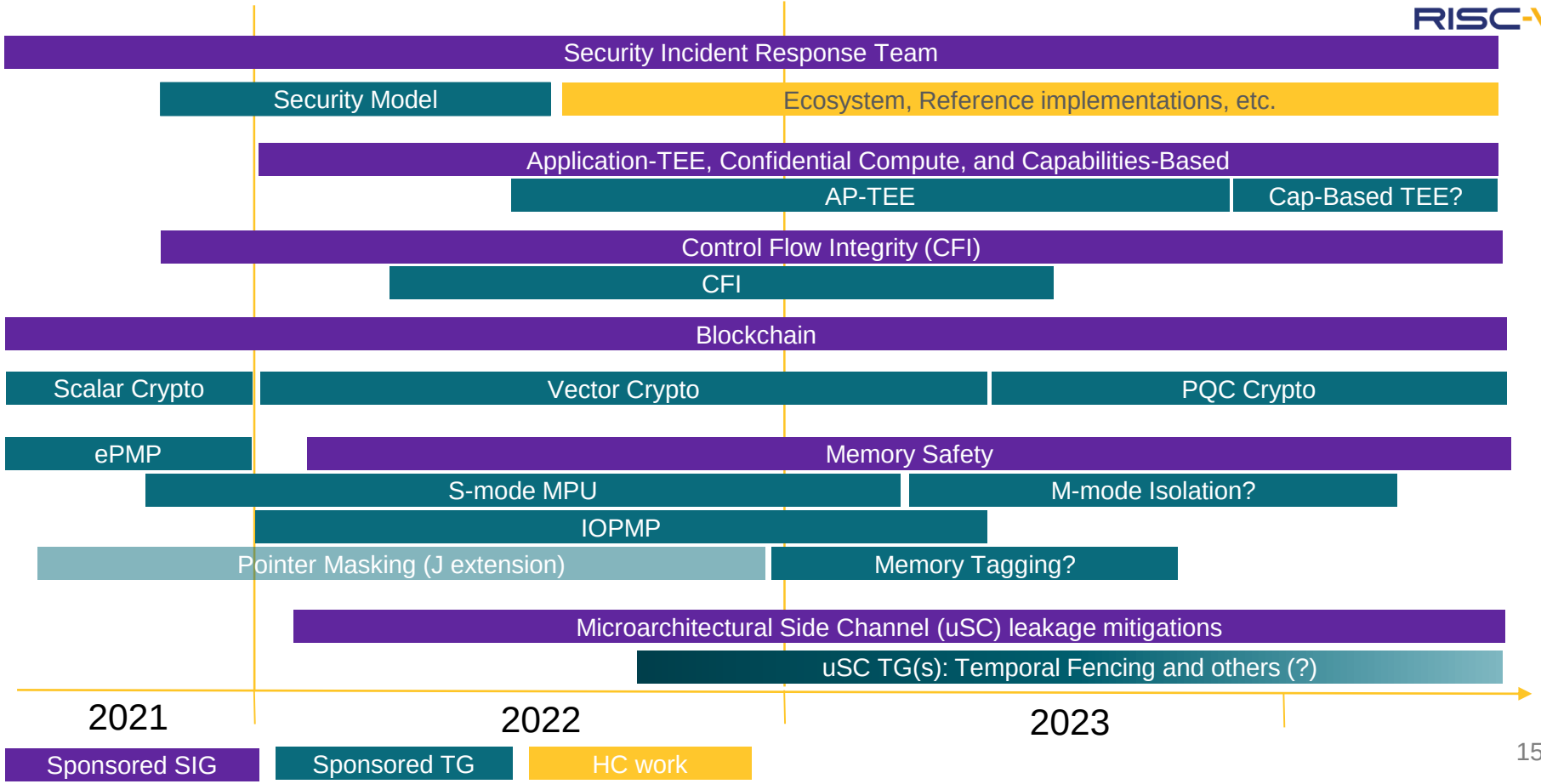
- Lightweight TEE
  - Potential Memory isolation scheme for small M/U systems.
  - Additional context to M mode
- Capability Based Security
  - CHERI

SIRT

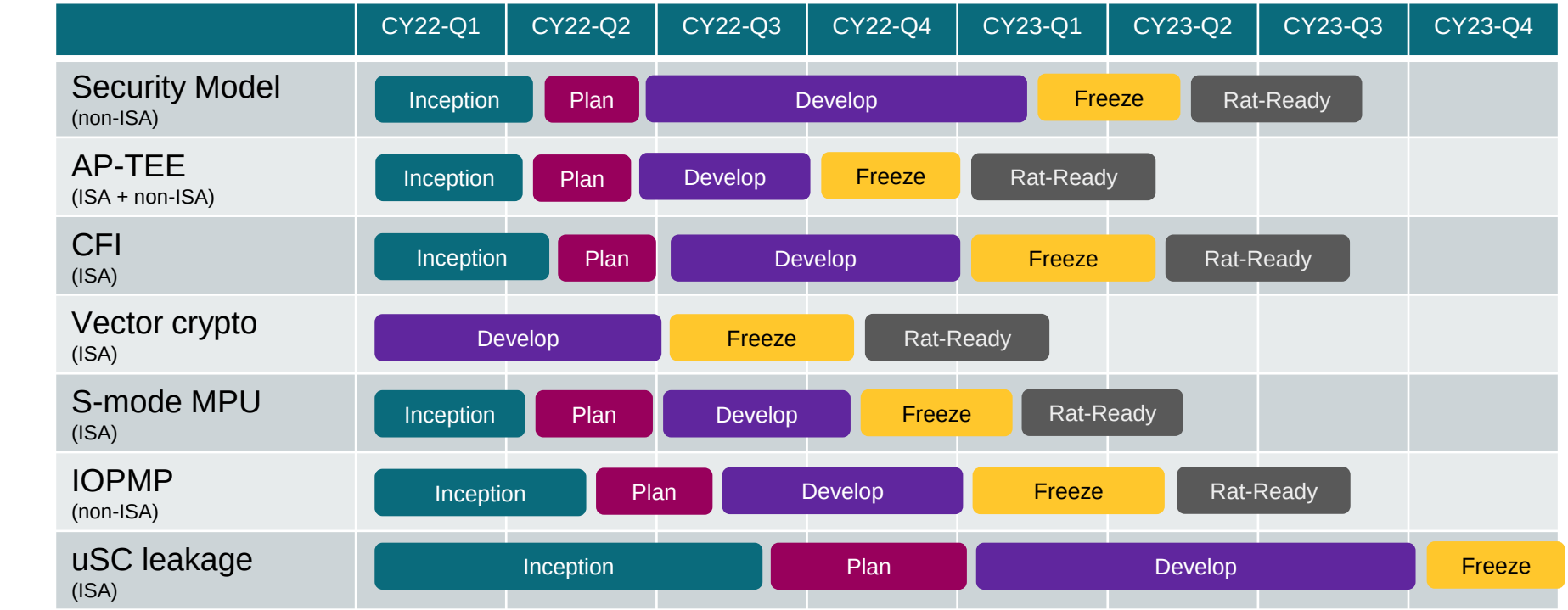
- Ensure continuity of the RISC-V Security Incident Response Team (SIRT)
- Institute and manage a responsible disclosure process
- Triage incoming security disclosures
- Maintain a catalogue of security issues

Status & Roadmap

Security HC - Roadmap



Specification Plan



RISC-V Security 5 year horizon

- Platform Security Model outlining RISC-V security capacities and system's integration
- Tools and Software support for RISC-V security capabilities
- Protection against side-channel information leakage at the hardware level
- Robustness capabilities to prevent malicious manipulation of e.g., code execution flows
- Cryptography support for small to large devices, including Post-Quantum Crypto
- Memory isolation and Trusted Execution Environments to securely separate applications from each other
- Support for Confidential Compute and Capability based models to enhance application and data privacy
- Blockchain technology on RISC-V based systems

We need your help:

Security@lists.riscv.org