Building an Open HPC Ecosystem
Special Interest Group for High Performance Computing

John D. Davis, Chair, SIG-HPC
Overview

- The HPC Vision
- SIG HPC Goals
- SIG HPC Activities
- RISC-V HPC Research in Europe
- Concluding thoughts
Open Ecosystem HW/SW Co-Design

- GROMACS, NAMD, Quantum Espresso, ...
- FFTW, BLAS, SLEEF, ...
- SLURM, xCat, MPICH, OpenMP, ...
- GCC, LLVM, GDB, Binutils, ...
- Linux, FreeBSD, ...

Applications
Libraries/Platforms
Schedulers
Compiler/Toolchain
OS
HW Systems
CPUs/GPUs/ASICs

https://github.com/riscv/riscv-software-toolchain
https://github.com/riscv-test/riscv-hpc
Europe can lead the way to a completely open SW/HW stack for the world
RISC-V provides the open source hardware alternative to dominating proprietary non-EU solutions
Europe can achieve complete technology independence with these foundational building blocks
Currently at the same early stage in HW as we were with SW when Linux was adopted many years ago
RISC-V can unify, focus, and build a new microelectronics industry in Europe.

OPEN

GROMACS, NAMD, WRF, VASP, etc.
Applications
OpenMP
Libraries/Platforms
COMPS
Schedulers
LLVM
Compiler/Toolchain
Linux
OS
OCP
HW Systems
RISC-V
CPUs/GPUs/ASICs
HPC [Open] Source Software for Open Source Hardware

| Applications: GROMACS, WRF, NAMD, ALYA, CP2K, ... |
| SW Libraries: OpenBLAS, BLIS, FFTW, ... |
| Middleware: OneDNN, TF, Apache Spark, COMPS, ... |
| Runtime & Schedulers: SLURM, DROM, MPI+OpenMP, TAMPI, DLB, ... |
| System SW: Linux, Drivers, Containers, ... |
| Toolchain: LLVM, Profiling, Optimization, & Performance tools ... |

General Purpose Processor

Accelerator/Embedded
SIG-HPC Vision & Mission: RISC-V: IoT to HPC

Vision:
The technical and strategic imperatives that guide the RISC-V ecosystem development to enable an Open HPC Ecosystem…

Mission:
…enable RISC-V in a broader set of new software and hardware opportunities in the High Performance Computing space, from the edge to supercomputers, and the software ecosystem required to run legacy and emerging (AI/ML/DL) HPC workloads.
SIG-HPC: An Open era of HPC!

- CPUs, Accelerators, other hardware units, and coprocessors
- Verification and compliance infrastructure and methodologies specific to HPC
- Alignment and engagement and IP enablement.
- RISC-V software ecosystem alignment
- Engage and represent RISC-V in compute intensive industry and academic events
- Identify key industrial and academic partners.
- Support global technology independence with a RISC-V ecosystem roadmap and partners
SIG-HPC Initiatives

- Guide and enable the community
  - Virtual Memory
    - SV57, SV57K, SV64, SV128
  - HPC SW & HW ecosystem & roadmap
  - Accelerators
  - ISA Extensions
  - **HPC Software Stack**
    - Starting with HPC Libraries
  - **New Announcement!**
HPC Software Testbed

John Leidel, Ph.D.
Tactical Computing Labs, RISC-V Technology HC Chair & SIG-HPC Co-Chair
Categories of Software

Applications
- HMMER
- WRF
- BLAST
- GROMACS
- VASP
- Espresso
- (...)

Benchmarks
- Linpack
- HPCG
- Graph500
- Mantevo
- BOTS
- NASPB
- (...)

Tools
- xCat
- Singularity
- Spack
- OpenMPI
- OpenSHMEM
- GCC
- LLVM
- (...)

Libraries
- FFTW
- MUMPS
- ARPACK
- Trilinos
- SLEEF
- BLAS
- (...)
HPC Software Testbed

- We are working with the RISC-V International group to drive requirements for adjacent working groups
- RISC-V HPC Tests
  - HPC-centric software test suite
  - Multi-version compiler centric: GCC, LLVM
  - Using each compiler, we cross compile each target library, benchmark and application suite for RISC-V compatibility
# HPC Software Testbed: riscv-test.org

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<th>W</th>
<th>Name</th>
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<th>Last Failure</th>
<th>Last Duration</th>
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<td>7 mo 9 days - #1</td>
<td>37 min</td>
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<td>5 mo 21 days - #36</td>
<td>2 hr 47 min</td>
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</table>
HPC Software Testbed: Public Results

Stage Logs (Build stage:/jenkins/workspace/llvm-project-12.0.1/tests/lib/openblas-master.sh)

Shell Script -- bash /jenkins/workspace/llvm-project-12.0.1/tests/lib/openblas-master.sh (self time 24min 11s)

rm -f linktest
make[1]: Leaving directory '/jenkins/workspace/llvm-project-12.0.1/build/openblas-master.sh-SRC/exports'

OpenBLAS build complete. (BLAS CBLAS)

OS  ... Linux
Architecture ... riscv64
BINARY  ... 64bit
C compiler  ... CLANG {cmd & version : clang version 12.8.1}
Library Name  ... libopenblas_riscv64_genericpc-r0.3.17.dev.a (Multi-threading; Max num-threads is 8)

To install the library, you can run "make PREFIX=/path/to/your/installation install".

make -j 8 -f Makefile.install install
Public Test Harness

- The results are public!
  - [https://riscv-test.org/](https://riscv-test.org/)

- The test harness has been created in a public Github repo
  - [https://github.com/riscv-test/riscv-hpc](https://github.com/riscv-test/riscv-hpc)

- The harness includes a set of template scripts for each test
  - Each test pulls its own source code (archive or Git repo)
  - Unpacks the source, configures it and builds it
  - Adding tests is as simple as adding scripts to the Github repository

- The top-level harness provides common access to:
  - Directory structures
  - Compiler paths
  - Compiler flags

- Pull requests are encouraged!
InfiniBand on RISC-V

- Infiniband working on RISC-V Unmatched Board
  - System boots and the card shows up in the necessary configuration points
    - standard kernel drivers without manual intervention
  - Running Ubuntu 21.04 and 21.10 with factory kernels
    - 21.04+ on RISC-V even offers all the IB tools via the standard apt repositories
    - Subnet manager has the normal issues

`ibstat` shows this (for one of the two ports):
CA 'mlx4_0'
CA type: MT4099
Number of ports: 2
Firmware version: 2.40.7000
Hardware version: 1
Node GUID: 0x7cfe9003009ece10
System image GUID: 0x7cfe9003009ece10
Port 1:
State: Active
Physical state: LinkUp
Rate: 40
Base lid: 0
LMC: 0
SM lid: 0
Capability mask: 0x00010000
Port GUID: 0x7efe90fffe9ece10
Link layer: Ethernet
ConnectX3 Infiniband not out of the Box

- The latest Linux kernels are shipped with sufficient drivers to run most of the IB stack. This includes the basic drivers and IP over IB.
- The latest RISC-V kernels lack RDMA driver support for Mellanox devices.
- You can download the source for the RDMA drivers directly from Mellanox, but due to some recent kernel changes, they do not build on RISC-V Linux.
- This may be solved by moving to more recent IB devices (ConnectX-4+), but there is also a planned fix coming in forthcoming kernel releases.
RISC-V BoF @ ISC ’22

- Creating an Open HPC Ecosystem with RISC-V
- Monday, May 30, 2022 2:30 PM to 3:30 PM
  - David Donofrio, Tactical Computing Labs
  - Doug Norton, Inspire Semiconductor
  - Michael Wong, Codeplay Software
    - Also leads the RISC-V Datacenter Group
- Discuss the SW/HW RISC-V Ecosystem
  - 20 minutes of presentation/40 minutes of discussion
- Come join us for the conversation
RISC-V @ SC’22 in Dallas ???
November 13-18
Coming Soon: SUPERcomputing Risc-V LAB
SUPER-V @ BSC

- Enabling the development of the HPC ecosystem for RISC-V based systems
- Variety of systems
  - RISC-V clusters running HPC software stack (i.e., Unmatched cluster)
  - RISC-V Experimental/research platforms for vector architectures
    - FPGA-based system
    - Software emulators
    - Hybrid software/hardware emulators
- HPC Software ecosystem development
- And more…
- Access information coming soon…
  - Easybuild and Gentoo first success story
SUPER-V@ BSC

- **Clusters:**

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<th>Board</th>
<th>OS</th>
<th>Details</th>
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<tbody>
<tr>
<td>PolarFire</td>
<td>Fedora</td>
<td>4 cores w/ 2 GB</td>
</tr>
<tr>
<td>BeagleV</td>
<td>Fedora</td>
<td>2 cores w/ 8 GB</td>
</tr>
<tr>
<td>Unmatched</td>
<td>Fedora/Ubuntu</td>
<td>4 cores w/ 16 GB</td>
</tr>
<tr>
<td>Allwinner D1</td>
<td>Fedora</td>
<td>1 core w/ 2 GB</td>
</tr>
<tr>
<td>(Vector extension)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Board OS Details**
  - PolarFire: Fedora, 4 cores w/ 2 GB
  - BeagleV: Fedora, 2 cores w/ 8 GB
  - Unmatched: Fedora/Ubuntu, 4 cores w/ 16 GB
  - Allwinner D1 (Vector extension): Fedora, 1 core w/ 2 GB

- **Emulators:**
  - A RISC-V soft vector core running in an FPGA.
  - The Vehave RISC-V emulator on top of QEMU
  - The Vehave RISC-V emulator on top of a native RISC-V core

- **RISC-V Software Stack:**
  - **Linux, SLURM**
  - **Compilers:**
    - go/1.17
    - openmpi/fedora/4.1.1_gcc10.3.1
    - llvm/EPI-0.7-development
    - openmpi/ubuntu/4.1.1_gcc10.3.0
    - llvm/EPI-development
    - python/fedora/2.7.16
  - **Tools**
    - extrae/3.8.3
    - papi/6.0.0
    - perf/5.11.10
    - singularity/3.8.2
  - **Libraries**
    - boost/1.77.0
    - glibc/fedora/2.33
    - openBLAS/0.3.15
    - fftw/3.3.9_gcc10.3.1_ompi4.1.1
    - libunwind/git
    - openBLAS/0.3.17
Building Open European HPC CPUs & Accelerators

Closed + Open

Research

Open

* Many more projects & products to come!
Recap: RISC-V in EU RESEARCH

- 2019: What is Open Source Hardware??
- 2020: Open Source Hardware
- 2021: RISC-V? Roadmap?
  - November roadmap report
  - Horizon Europe Work Programme 2021-22:
    - Open Source Hardware (OSH) appears 6 times
    - CSA Roadmap
- 2022: Build RISC-V!!!
  - KDT JU Work Programme 2021 v13:
    - RISC-V appears 25 times / OSH appears 2 times
  - EU Chip Act (collection of documents)
    - RISC-V and OSH appears 5 each
  - New KDT Call: Call 2022-1 Topic 3: Focus topic on Design of Customisable and Domain Specific Open-source RISC-V Processors (IA)
- More to come! (EuroHPC, KDT/Chip JU, etc.)
Building an Open HPC Ecosystem with RISC-V

- HPC requires customized hardware solutions for many HPC domains
- HPC is tackling grand challenges that benefit from the Global Technology ecosystem
- HPC is on the technology leading edge

- An Open ISA complements Open Source Software and combines to create an open Ecosystem

- RISC-V accelerates innovation both in Research and Industry
- The RISC-V community and ecosystem are rapidly growing
You Can Help

- Get involved in SIG HPC
- [https://lists.riscv.org/g/sig-hpc](https://lists.riscv.org/g/sig-hpc)
- Subscribe:
  - Send email to: sig-hpc+subscribe@lists.riscv.org
- Monthly meetings
  - 3rd Thursday of the month @ 16:00 CET
  - Next meeting is May 19, 2022
Thank you

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