SiFive’s founders are the same UC Berkeley professor and PhDs who invented and have been leading the commercial implementation of the RISC-V Instruction Set Architecture (ISA) since 2010.
SiFive in a nutshell

- 450 employees (and hiring)
- 15 offices
- 16+ SiFive CoreIPs
- 120+ design wins
Massive Growth in Devices & Data

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Compute Needs Are Changing

- e.g., machine learning

But, CPUs are not getting faster!

Source: Medium, Entering the world of Machine Learning

Based on SPECIntCPU. Source: John Hennessy and David Patterson, Computer Architecture: A Quantitative Approach, 6/e, 2018
Hardware Trends: Custom Hardware To The Rescue!

But, custom chip development costs are too high!

GPUs
Custom Chips (e.g., Google TPU)
Embedding Intelligence: From the Edge to the Cloud

U Cores
64-bit Application Processors

S Cores
64-bit Embedded Processors

E Cores
32-bit Embedded Processors

Intelligent Edge

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SiFive Core IP RISC-V Configurable Cores

<table>
<thead>
<tr>
<th>7 Series</th>
<th>32-bit embedded cores</th>
<th>64-bit embedded cores</th>
<th>64-bit application cores</th>
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<tr>
<td><strong>E Cores</strong></td>
<td><strong>S Cores</strong></td>
<td><strong>U Cores</strong></td>
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<tr>
<td><strong>E7 Series</strong></td>
<td><strong>S7 Series</strong></td>
<td><strong>U7 Series</strong></td>
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<tr>
<td>E76-MC Quad-core 32-bit embedded processor</td>
<td>S76-MC Quad-core 64-bit embedded processor</td>
<td>U74-MC multicore for U74 cores and one S76 core</td>
<td></td>
</tr>
<tr>
<td>E76 High performance 32-bit embedded core</td>
<td>S76 High-performance 64-bit embedded core</td>
<td>U74 High performance Linux-capable processor</td>
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</tbody>
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<tr>
<th>3/5 Series</th>
<th>Efficient performance: 5-6-stage, single-issue pipeline</th>
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<tbody>
<tr>
<td><strong>E3 Series</strong></td>
<td><strong>S5 Series</strong></td>
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<tr>
<td>E34 E31 features + single-precision floating point</td>
<td>S54 S51 features + single-precision floating point</td>
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<tr>
<td>E31 Balanced performance and efficiency</td>
<td>S51 Low-power 64-bit MCU core</td>
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<th>2 Series</th>
<th>Power &amp; area optimized: 2-3-stage, single-issue pipeline</th>
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<tr>
<td><strong>E2 Series</strong></td>
<td><strong>S2 Series</strong></td>
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<tr>
<td>E24 E21 + single-precision floating point</td>
<td>S21 No 64-bit Cortex equivalent</td>
</tr>
<tr>
<td>E21 User Mode, Atomics, Multiply, TIM</td>
<td>Area-efficient 64-bit MCU core</td>
</tr>
<tr>
<td>E20 Our smallest, most efficient core</td>
<td>No 64-bit Cortex equivalent</td>
</tr>
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</table>
SiFive Cloud Services

- SiFive Core Designer
- Click to configure a RISC-V Core!
- RTL download in 24hrs!
- Core IP configured to your needs!
Quarterly updates

- SiFive delivers IP and product updates on a quarterly basis
- Q3 Update includes Nexus 5001 trace encoders
- SiFive Freedom Studio support
- Open Source RISC-V Trace Decoder now on github
Learn More - SIFIVE.COM

• HiFive Unleashed
  – Quad Core Linux Capable CPU
  – Available via CrowdSupply

• SiFive World Tour
  – 50-City Tour
  – SiFiveTechSymposium.com
SiFive Commercial Success

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SoC security best practices

- Avoid fragmented security solutions
- Get rid of legacy security
- Get a Root-of-Trust
- Improve auditability
RISC-V SoC needs more security

- Scalable architecture
- Enhanced isolation
- Finer grained controls
- System level security
Join SiFive CTO, Yunsup Lee, and Security Director, Dany Nativel, for the latest innovations and updates on SiFive architectures!